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Assembly and Characterization of Cabled RODs During Production at CERN

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Abstract

In this document we summarize the test setups and characterization procedures of the ~700 cable ROD structures assembled at CERN. After the assembly and the electrical characterization tests, cabled RODs will be delivered to FNAL where detector modules will be mounted on them. Two basic tests on cabled RODs are envision at CERN: electrical characterization tests and functionality tests. The electrical tests will check the electrical continuity of the service and cable connections along the bus. The functional tests will assure the readout operation of the ROD as a whole readout unit. The functionality tests can also be used to characterize final RODs with detector modules both at FNAL and at CERN.
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1. Introduction
The TOB silicon detector modules, the services, the cables and the electronics needed for the functioning of the detectors are installed into independent supporting elements, the RODs. The RODs are compact units, easy to handle and mechanically robust, where the detectors and the services can be tested in stand-alone mode for all their functionality.

The main load carrying elements of the ROD are carbon fiber C-profiles interconnected with carbon fiber cross-links that guarantee the integrity of the structure. The services are arranged along straight paths inside the RODs, or on top of the modules, to minimize the assembly work, costs, and failure risk. One of the ROD ends serves as a miniature patch panel where all cables and service lines end. The optical fibers are joined via MT connectors at the end of the ROD. The gas inlet and outlet pipes are realized in stainless steel and run along the two C-profiles of the ROD. They are tied, through an aluminum heat removal plate, to the top surface of each module positioning insert. The last part of ROD assembly is the mounting of the silicon detector modules on cabled RODs.

Cabled RODs will be assembled and test during production at CERN. They will then be shipped to FNAL where the last stage of assembly (mounting of detector modules) will be done. Final RODs will be exercised with basic functionality tests, run in cold (burn-in) and shipped back to CERN [1].

In this paper we describe the characterization procedures on cabled RODs at CERN. There are two basic tests planned on cabled RODs: electrical characterization tests and functionality tests.

2. ROD Assembly
The support structure of RODs are made from carbon fiber/vinylester composite profiles and aluminum inserts. An electrical ROD is assembled in three main steps:

1. The carbon fiber pieces are glued together to form the main support structure frame of the ROD. The precision of the final resulting structure is about 1 mm in all dimensions.

2. The detector module support inserts and ROD support inserts, together with the cooling pipe, are then glued to the carbon fiber frame. The detector module support inserts define parallel planes on which the detector modules are mounted. The ROD support inserts define a plane which is planar to the detector support planes on the ROD. The ROD support inserts are then the elements that make the contact to the supporting wheel and align the ROD in the TOB assembly.

3. The ROD is then cabled by mounting the mother cable, high voltage wires, interconnect cards, control module (CCUM board), and opto-hybrids with the optical fibres. The cables terminate in connectors at the end of the ROD.\(^1\)

Assembly steps 1 and 2 above will be done in Helsinki together with other tests like pipe tightness, mechanical integrity (temperature cycling) and cooling performance measurements. Step 3 will be carried out at CERN. Figure A1 shows a ROD frame structure equipped with the interconnect cards (ICC) and one module frame.

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\(^1\) See http://jvalls.home.cern.ch/jvalls/rod_assembly.htm
3. Cable ROD Components

3.1. ROD Frames
The ROD frames include the Carbon fiber profile, the Aluminum inserts and the cooling pipe. ROD frames will come with a small 2D bar code (with a Dice-2 tag) glued to the frames in Helsinki. There are four types of ROD frames:

SS Type-H  SS Type-L  DS Type-H  DS Type-L

SS and DS stand for single-sided and double-sided RODs respectively. On ROD frames one can always verify the correspond to SS or DS by measuring the diameter of the cooling pipe. It is 2.2 mm in SS and 2.5 mm in DS RODs. RODs of type H refer to the module closest to Z=0 being on the top side of the ROD, seen from outside of the barrel. RODs of type L refer to the module closest to Z=0 being on the bottom side of the ROD seen from outside of the barrel. The positions of the inserts supporting modules 3 and 5 make the difference between L type and H type. A verification measurement is easy with an ordinary ruler.

There will be a total of 760 ROD frames (688 used and 72 spares).

3.2. IC Bus (ICB)
The ICB (Interconnect Bus) include the high voltage and low voltage cables and adapter connectors. There will be a total of 4 different types of ICBs, depending on whether it is a DS ICB (8 HV wires routed) or a SS ICB (6 HV wires routed), and whether it is a type-H (module 3/5 connector in position H) or a type-L (module 3/5 connector in position L).

ICBHDS has the module 3/5 connector in position H and has 8 HV wires routed.
ICBLDS has the module 3/5 connector in position L and has 8 HV wires routed.
ICBHSS has the module 3/5 connector in position H and has 6 HV wires routed.
ICBLSS has the module 3/5 connector in position L and has 6 HV wires routed.

<table>
<thead>
<tr>
<th>TYPE</th>
<th>USED</th>
<th>SPARES</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICBHDSH</td>
<td>90</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>ICBLDH</td>
<td>90</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>ICBHS</td>
<td>254</td>
<td>26</td>
<td>280</td>
</tr>
<tr>
<td>ICBHS</td>
<td>254</td>
<td>26</td>
<td>280</td>
</tr>
<tr>
<td>Total</td>
<td>688</td>
<td>72</td>
<td>760</td>
</tr>
</tbody>
</table>

One could further consider four more types of ICBs according to the type of temperature or humidity sensor routed along the bus. In this way we have:

ICBHDSH has the module 3/5 connector in position H - 8 HV wires routed - Humidity sensor.
ICBHDSLST has the module 3/5 connectot in position H - 8 HV wires routed - Temperature sensor.
ICBLDSH has the module 3/5 connector in position L - 8 HV wires routed - Humidity sensor.
ICBLDST has the module 3/5 connector in position L - 8 HV wires routed - Temperature sensor.  
ICBHSSH has the module 3/5 connector in position H - 6 HV wires routed - Humidity sensor.  
ICBHSSST has the module 3/5 connector in position H - 6 HV wires routed - Temperature sensor.  
ICBLSSSH has the module 3/5 connector in position L - 6 HV wires routed - Humidity sensor.  
ICBLSSST has the module 3/5 connector in position L - 6 HV wires routed - Temperature sensor.  

The number and type of ICB cards to be assembled during production are shown in the table below:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>USED</th>
<th>SPARES</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICBHDSH</td>
<td>15</td>
<td>3</td>
<td>18</td>
</tr>
<tr>
<td>ICBHDDST</td>
<td>75</td>
<td>8</td>
<td>83</td>
</tr>
<tr>
<td>ICBLDSH</td>
<td>15</td>
<td>3</td>
<td>18</td>
</tr>
<tr>
<td>ICBLDST</td>
<td>75</td>
<td>8</td>
<td>83</td>
</tr>
<tr>
<td>ICBHSSH</td>
<td>31</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>ICBHSST</td>
<td>223</td>
<td>21</td>
<td>224</td>
</tr>
<tr>
<td>ICBLSSH</td>
<td>31</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>ICBLSSST</td>
<td>223</td>
<td>21</td>
<td>224</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>688</strong></td>
<td><strong>72</strong></td>
<td><strong>760</strong></td>
</tr>
</tbody>
</table>

There will be a total of 760 ICBs (688 used and 72 spares).

3.3. **IC Cards (ICC)**

There are four types of ICCs (Interconnect Cards): DS_ICC1, DS_ICC2, SS_ICC1, and SS_ICC2. Around 10% of the total ICCs produced will be used as spares. The number and types of each ICC cards are shown in the following table:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>USED</th>
<th>SPARES</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS_ICC1</td>
<td>360</td>
<td>40</td>
<td>400</td>
</tr>
<tr>
<td>DS_ICC2</td>
<td>360</td>
<td>40</td>
<td>400</td>
</tr>
<tr>
<td>SS_ICC1</td>
<td>1016</td>
<td>104</td>
<td>1120</td>
</tr>
<tr>
<td>SS_ICC2</td>
<td>1016</td>
<td>104</td>
<td>1120</td>
</tr>
</tbody>
</table>

3.4. **CCUM Modules**

There will be basically three different types of CCUMs in the TOB:

- **CCUM1**: first ROD of a control loop.
- **CCUM2**: second ROD of a control loop.
- **CCUM**: other ROD in the control loop.

**CCUM1** will be configured to control the transmitters of the DOHM of the primary loop of the control ring. **CCUM2** will be configured to control the transmitters of the DOHM of the secondary loop of the control ring. **CCUM** will be configured to bypass the transmitters control lines of the DOHM.

The total number of available addresses in the CCU IC chip is 128 (7 bits). Address 0 is used by the FEC, which is part of the control loop it is associated with. The total number of CCUMs (or RODs) in the TOB is 688 plus 72 spares. There will be a total of 46 control loops in each of the two TOB barrels. Each control loop handles between 4 and 10 RODs (or CCUMs). Each layer of the TOB has a different number of control loops (either 7 or 8 control loops, depending on the layer). CCUMs in a control loop must have different addresses. See Figure A3.

The following table shows the number and type of CCUMs with their addresses to be build during production:

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Spares</th>
<th>Total</th>
<th>CCU Address</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CCUM1</strong></td>
<td>Total number of control loops: 46</td>
<td>10</td>
<td>102</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Used = 2 x 46 = 92</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUM2</strong></td>
<td>Total number of control loops: 46</td>
<td>10</td>
<td>102</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>Used = 2 x 46 = 92</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUM</strong></td>
<td>Layers 1-2 type H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUML12H</strong></td>
<td>Total RODs: 48+42=90</td>
<td>0</td>
<td>60</td>
<td>3 → 62</td>
</tr>
<tr>
<td></td>
<td>Control loops: 8+7=15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used = 90–15 x 2 = 60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUML12L</strong></td>
<td>Layers 1-2 type L</td>
<td></td>
<td>60</td>
<td>3 → 62</td>
</tr>
<tr>
<td></td>
<td>Total RODs: 48+42=90</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Control loops: 8+7=15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used = 90–15 x 2 = 60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUM</strong></td>
<td>Layers 3-4 type H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUML34H</strong></td>
<td>Total RODs: 54+60=114</td>
<td>10</td>
<td>94</td>
<td>3 → 96</td>
</tr>
<tr>
<td></td>
<td>Control loops: 7+8=15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used = 114–15 x 2 = 84</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUML34L</strong></td>
<td>Layers 3-4 type L</td>
<td></td>
<td>94</td>
<td>3 → 96</td>
</tr>
<tr>
<td></td>
<td>Total RODs: 54+60=114</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Control loops: 7+8=15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used = 114–15 x 2 = 84</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUM</strong></td>
<td>Layers 5-6 type H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUML56H</strong></td>
<td>Total RODs: 66+74=140</td>
<td>16</td>
<td>124</td>
<td>3 → 126</td>
</tr>
<tr>
<td></td>
<td>Control loops: 8+8=16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used = 140–16 x 2 = 108</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CCUML56L</strong></td>
<td>Layers 5-6 type L</td>
<td></td>
<td>124</td>
<td>3 → 126</td>
</tr>
<tr>
<td></td>
<td>Total RODs: 66+74=140</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Control loops: 8+8=16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used = 140–16 x 2 = 108</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
According to the previous table, the following number of CCUM with addresses will be assembled:

<table>
<thead>
<tr>
<th>CCUM Type</th>
<th>Address</th>
<th>Number to be assembled</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCUM1</td>
<td>1</td>
<td>102</td>
</tr>
<tr>
<td>CCUM2</td>
<td>2</td>
<td>102</td>
</tr>
<tr>
<td>CCUM</td>
<td>3 → 62</td>
<td>6×60 = 360</td>
</tr>
<tr>
<td>CCUM</td>
<td>63 → 96</td>
<td>4×(94-60) = 136</td>
</tr>
<tr>
<td>CCUM</td>
<td>97 → 126</td>
<td>2×(124-94) = 60</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>760</strong></td>
</tr>
</tbody>
</table>

After assembly of the ICB, ICCs and CCUM on the Carbon fiber ROD profiles we will have 18 different types of electrical cable RODs: either DS or SS, type H or type L, and with CCUM1, CCUM2 or CCUM boards.

4. Electrical Tests

The goal of the electrical integrity tests is to verify during production that the cabling and the connections in the cabled RODs are fully functional.

4.1. Electrical Tests of Single Components

4.1.1. Electrical Tests of ICB, ICC, Cables and Connectors

Individual tests on the ROD Interconnect Bus (ICB), ROD Interconnect Cards (ICC), ROD cables and adapter card connectors will be done in the industry. These tests will consist on electrical signal continuity, pin to pin and vias continuity.

4.1.2. Electrical Tests of CCU Module (CCUM)

In the cabled ROD (without the Silicon detector modules) the most complex component is the CCU module (CCUM). The CCUM carries the CCU_25 IC chip, LVDS_Buf chips and DCU chips, and it cannot be tested with a conventional tester (e.g. Bed of nail tester or similar type of tester). In the following Sections a test setup is proposed to be used either at the industry (to check the assembled CCUM boards) and at CERN for final tests and debugging. The test setup is designed for simplicity and efficiency and it will cover more than 95% of the module functionality by direct or indirect testing.

Components Required for the Setup:

1. PMC-FEC.
2. Test board PCB (called Test Bed Card). This board will contain all the required hardware for the test setup and will serve as the interface board between the FEC, PC and the
CCUM. The mechanical assembly for this board, power supply and connectors is shown in Figure 1.

3. PC Power supply. A standard PC power supply used to power up the test setup and the CCU module under test.

4. PC. One computer will be required with at least one PCI slot empty for the FEC and the control and test software.

5. Test software. This software will be capable to operate in single steps and in one go test modes. The results can be stored in a log file with CCUM identification. An example of the user interface program used for the CCUM tests is shown in Figure 2.

6. Electrical CCUM Connections To Be Tested

The electrical CCUM connections to be tested with the CCUM test setup are summarized below. Figure 3 shows the layout of the CCUM card with the TOB ROD control input and output connectors.

1. Control Ring Connections:
   To implement the redundancy architecture of the CCUM (control ring), the FEC and all CCUM modules have two sets of input ports and two sets of output ports. These ports are called A and B ports. The control ring connections to be tested include the data and clock input/output lines for both ports (A and B). Other control ring connections to be tested include the two input and two output I2C lines (I2C channel 15 in the CCU25) to program the primary (port A) and secondary (port B) transmitters of the DOHM (Digital OptoHybrid Module).

   i. Clk1A & Dat1A   Clock and data inputs to CCUM
   ii. Clk1B & Dat1B (control input connector)
   iii. Clk2B & Dat2B
   iv. Clk2A & Dat2A
   v. Clk2B & Dat2B  Clock and data outputs from CCUM
   vi. Clk3B & Dat3B (control output connector)
   vii. Sdta + Sclk_1 for TxA
   viii. Sdta + Sclk_2 for TxB I2C clock and data lines for programming
   ix. Sdta + Sclk_2 for TxB of DOHM
   x. Sdta + Sclk_n for TxA
   xi. Ground lines
   xii. V250 lines
   xiii. Reset lines

2. ROD IC Bus (ICB) Interface Connections:
   The ROD bus interface connections to the CCUM board to be tested include the 12 I2C lines used to address the front-end modules of the ROD (CCU I2C channels 0-11), the system clock lines of the bus and the 6 reset lines and 2 back-plane pulse lines. The CCUM receives four pairs of lines from the ROD bus which measure two temperatures from the Silicon modules (SiTmp1, SiTmp2) and two temperatures from the ROD (LiqTmp, AirTmp). These four lines are available in the CCUM. One out of the two Silicon temperatures, and one out of the ROD temperatures can be driven and readout by the DCU sitting on the CCUM.
i. I2C Clock (12 lines) & data lines (12 lines).
ii. System clock lines.
iii. Reset (6 lines) and back plane pulse lines (2 lines).
iv. ROD and Silicon temperature lines (8 lines). Only those which are strapped on the CCUM will actually be tested.
v. ROD power lines (V250 lad, V125 lad).
vi. Ground lines (24 lines).

3. Functional Testing of Chips:

i. CCU_25
ii. LVDSMUX
iii. LVDSBUF
iv. DCU
v. Humidity Sensor (if it is there)

Tests to be performed:

1. V250 and ground input and output lines (with power off):

The first step in the testing sequence will be to test the power and ground lines. For this purpose four test point connectors are provided on the test setup, which are:

- J7: provides access to all the individual ground pins of the CCUM ring output connector (31 pin binder).
- J8: provides access to all the individual ground pins of the CCUM ring input connector (31 pin binder).
- J9: provides access to all the individual 2.5 V pins of the CCUM ring input/output connectors (31 pin binder).
- J10: provides access to all the individual ground pins of the CCUM IC bus output connector (80 pin NAIS connector).

The steps for the test are the following:

- The power to the CCUM and test setup should be kept off.
- For testing the validity of the soldering of the ground lines and the connectivity through the PCB traces, a matrix-like scan can be performed by using the connectors J7 and J8 as the rows, and connector J10 as the columns of the matrix.
- Activate all the rows one by one and measure the resistance with all the columns one by one.
Repeat step c) for all the rows.

For testing the validity of the soldering of the 2.5 V lines and the connectivity through the PCB traces, a matrix-like scan can be performed by using pins 1, 3, 5, and 7 of \textbf{J9} connector as the rows, and pins 9, 11, 13, and 15 of \textbf{J9} connector as the columns of the matrix.

Activate all rows one by one and measure the resistance with all the columns one by one.

Repeat step f) for all rows.

There are connectors provided to access the power and ground lines. The firm mounting the components will perform the tests. However, it can also be integrated with the test setup by using a standard DAQ card (with at least 36 IO lines) in the same PC being used for the rest of tests.

Details are given in Figure 4.

2. \textbf{Control ring test (with power on)}:

i. For the control loop there are three input and three output lines to and from the CCUM (ports A and B), named as:

- Input:
  \begin{itemize}
  \item Clk1A, Clk1B, Clk2B
  \item Dat1A, Dat1B, Dat2B
  \end{itemize}

- Output:
  \begin{itemize}
  \item Clk2A, Clk2B, Clk3B
  \item Dat2A, Dat2B, Dat3B
  \end{itemize}

ii. The Dat and Clk (2B) lines make a loop between the CCUM input and output connector.

iii. To operate through either path of the control ring (port A or B) a simple arrangement is provided by using the LVDSMUX chip on the test setup main board and by using the select line coming from the FEC. This is necessary as the FEC does not provide two independent clocks (for port A and B).

iv. The differential Clk1A line goes to the two inputs of the LVDSMUX chip and it comes out on two outputs as either Clk1A or Clk1B.

v. The Dat1A line goes directly from the FEC connector to the CCUM input connector.

vi. The Dat1B line goes to Dat2B of the input connector of the CCUM and then it comes out from the CCUM output connector through the Dat2B line. From here it is routed back to the Dat1B input of the CCUM through the test setup main board.

vii. In this way not only both paths for the control signals are tested but also the redundant path.
3. **I2C lines and 4-parallel port A lines (PIOA) test (with power on):**

The 16 I2C channels of the CCU25 (clock and data lines) can be tested by multiplexing them one by one to an I2C slave chip placed on the test setup main board, for both read and write operations. Actually only I2C lines 0-11, 13, and 15 (all of them accessible in the CCUM) will be checked with these tests. I2C line 12 is not used, and I2C line 14 is tested later (DCU, ROD power lines and strapped sensors tests).

The selection lines of the multiplexer (bi-directional switch) are controlled through the parallel IO port A (PIOA) of the CCU25 (four independent byte PIO adapter channels are available in the CCU, PIO ports A, B, C and D). The 8 bits available with PIO port A of the CCU25 control the 6 reset lines and the 2 back-plane pulses sent through the ROD IC bus. In this way, by using four bits of the PIO port A (bits 0-3), four out of these six reset lines are also tested. The table below shows the I2C channel selection.

<table>
<thead>
<tr>
<th>PIOA3</th>
<th>PIOA2</th>
<th>PIOA1</th>
<th>PIOA0</th>
<th>I2C CHANNEL OF CCU</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>14</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>15</td>
</tr>
</tbody>
</table>

Details are shown in Figure 6.
4. **Reset in/out lines to CCUM test (with power on):**

The input/output CCU25 reset lines can be checked by sending a reset signal activated by the FEC. This signal, after passing through the input and output connectors of the CCUM will clear the data on the counter which is used for testing the clock lines (see the system clock lines test section). The path for the signal flow in order to check the reset line both in the input and output connectors of the CCUM is:

**Reset from FEC → CCUM Input → CCUM Output → To counter rest line**

To test the reset lines the following sequence is performed:

- Generate the clock enable pulse by writing 010 sequences to bit 7 of PIOA and then add a delay of 250 \( \mu \)sec.
- Enable the buffer to which the 8 least significant bits of the counter pass to the I2C slave parallel port.
- Enable I2C channel 0 on the I2C multiplexers.
- Read the counter output through I2C channel 0.
- Send the reset signal and perform the steps two to four above. If the value of the counter is zero both reset lines (input and output connectors) are ok.
- Otherwise either the input or the output connector has a bad soldering. To find it out:
  - Write some values to the DCU registers (different from the reset values).
  - Send the reset signal and read back the DCU register; if the values are the same as those for the reset values, then the reset signal is ok at the input connector of the CCUM.
  - Otherwise there is a bad soldering on the input connector or no signal is coming from the FEC.

Details are given in Figure 7.
5. System clock lines test (with power on):

This test is performed in order to check the two differential lines of the 40 MHz clock coming from the CCUM through the IC bus 80-pin NAIS connector. This differential signal is converted into single ended on the test board. It is then gated with a calibrated pulse into a counter. PIO port A bit 7 is used as the single shot section trigger to generate the gate pulse. The clock can also be verified indirectly through the operation of the DCU.

Note that:

- By generating a pulse (up to 200 µsec) through the single shot (triggered by the PIOA bit 7) the clock signal will enable the counter. When the pulse ends the counter stops.
- The pulse enabling the clock will be of width 200 µsec. During this period, the counter should show 4000 counts for a 40 MHz clock frequency.
- This count will be read through buffers via an I2C slave on the I2C lines of the CCUM.

The steps are then:

- Write 010 sequences to bit 7 of PIOA port and add a delay of 250 µsec.
- Enable the buffer to which the 8 least significant bits of the counter pass to the I2C slave parallel port.
- Enable I2C channel 0 on the I2C multiplexers.
- Read the counter output through I2C channel 0.
- If the count if 4000 ± 1 count the clock is ok.
- Otherwise, if the count is zero there is no clock. Then:
  1. Check the readout of the DCU for 2.5 and 1.25 Volts
  2. If they are ok then there is a problem with the soldering of the IC bus connector on the CCUM.
3. If they are not ok, either the LVDS Mux or the CCUM input cable has a soldering problem.
4. If none of these problems appear one should replace the CCUM with a working one and repeat the tests. If the same problem appears there is a problem with the FEC or FEC to test setup cable.
   - If the count from the counter is less than 4000 counts the procedure should be repeated 5 times and whether the count varies.
   1. Check the readout of the DCU for 2.5 and 1.25 Volts.
   2. If they are ok then there is a problem with the soldering of the IC bus connector on the CCUM.
   3. If they are not ok, either the LVDS Mux or the CCUM input cable has a soldering problem.
   4. If none of these problems appear one should replace the CCUM with a working one and repeat the tests. If the same problem appears there is a problem with the FEC or FEC to test setup cable.

Details are shown in Figure 7.

6. **DCU, ROD power lines and strapped sensors test (with power on):**

The DCU of the CCUM module will be tested for:
- I2C read/write operations (CCU I2C channel 14).
- V250 and V125 low voltage power lines of ROD.
- Strapped sensor lines.
- Reset line for the DCU.

The test flow will consist on:
- Initialize the DCU registers.
- Read the DCU channels which are connected to ROD 2.5 V and 1.25 V lines. If the values read are ok the test is succesful; otherwise the ROD IC bus connector on the CCUM fails (bad soldering) or there is some problem with the DCU (if both channels are not giving good reading).
- Initialize the DCU register and send a reset to the CCUM
- Read the DCU register; if they go back to the reset values of the DCU the reset line test is succesful. If the register keeps its initialized values and the master rest is ok (already tested), then there is a problem in soldering the DCU to the CCU.

Details are shown in Figure 8.

The flow of the test procedure is summarized in Figure 9.
4.2. Electrical Tests of Components in the Assembled ROD

The main goal of the electrical tests is to verify after the assembly and the cabling of each ROD the electrical continuity of those signals which can not be checked during the functional tests. These are:

\[
\begin{align*}
V250, V125, GND & \Rightarrow \text{from LVRAC to ICB} \\
PS250, MS250 & \Rightarrow \text{from ICB to LVRAC} \\
PS125, MS125 & \Rightarrow \text{from ICB to LVRAC} \\
V250\text{lad}, V125\text{lad} & \Rightarrow \text{from ICB to CCUM} \\
\text{SiTmp1A, SiTmp1B} & \Rightarrow \text{from ICB to HVRAC and to CCUM} \\
\text{SiTmp2A, SiTmp2B} & \Rightarrow \text{from ICB to HVRAC and to CCUM} \\
\text{LiqTmpA, LiqTmpB} & \Rightarrow \text{from ICB to LVRAC and to CCUM} \\
\text{AirTmpA, AirTmpB} & \Rightarrow \text{from ICB to LVRAC and to CCUM} \\
HVij & \Rightarrow \text{from HVRAC to MODULE i / DETECTOR j} \\
\text{ITHij+}, \text{ITHij-} & \Rightarrow \text{from HYBRID to DETECTOR in MODULE i / DETECTOR j} \\
\text{BckPls1} & \Rightarrow \text{from CCUM to DETECTORS in MODULES 1, 3 and 5} \\
\text{BckPls2} & \Rightarrow \text{from CCUM to DETECTORS in MODULES 2, 4 and 6}
\end{align*}
\]

ICB stands for ROD InterConnect Bus. LVRAC and HVRAC stands for Low Voltage ROD Adapter Card and High Voltage ROD Adapter Card respectively (see later). CCUM is the Communication and Control Unit Module. MODULE i (i=1,6) refers to any of the six modules housed in the ROD (see Figure A2). MODULE i / HYBRID j and MODULE i / DETECTOR j (i = 1,6, j = 1,2) are one of the 12 front-end hybrids and detectors that can be housed in a DS ROD (in a SS ROD j = 1).

The ROD is powered through the LV connector housed in the LVRAC (V250, V125 and GND). V250, V125 and GND are then distributed to modules through the Inter-Connect Cards (ICCs). The first goal of the electrical test is to check all the power (V250, V125) and ground (GND) connections between the LVRAC and the connectors to the front-end hybrids in the ICCs. Two pairs of sensing lines, PS250 and MS250 for V250 and PS125 and MS125 for V125, that from the ICB go to the multi-service cable through the LVRAC are also checked. The connection of V250 and V125 to the CCUM used to monitor the power supply voltages through the DCU housed in the CCUM itself are also checked.

The ROD IC bus has 8 high voltage lines which match the high voltage lines in the multiservice cable. Actually only 6 of these lines are used (the other 2 are spare lines). In DS RODs the line HVij serves the two detectors MODULE I / DETECTOR j (j = 1,2). In SS RODs it serves the detector MODULE i / DETECTOR 1 only.

The ICB also has 12 I2C lines connected to 12 of the 16 I2C output channels of the CCU25 housed in the CCUM. The line I2Cij is used to control MODULE i / HYBRID j. The ICB has also 6 reset lines (Rst1, Rst2, Rst3, Rst4, Rst5, and Rst6), one for each module, and 2 back-plane pulse lines (BckPls1 and BckPls2), one for modules 1, 3 and 5, and the other for modules 2, 4 and 6. These 8 lines come from the CCUM module through one of the four parallel input/output ports of the CCU25 chip (PIO channel A). The continuity of the 12 I2C lines, of the reset lines and of the clock lines (from CCUM to all the front-end hybrids) will also be tested giving useful guidelines together with the results of the functional tests for further debugging (if required).
The kapton HV cable of each TOB silicon detector module has three Murata thermistor probes. The two terminals of one of these thermistors can be connected through a jumper that seats on the Inter-Connect Card to two lines routed in the ICB. In the ROD IC bus there are two pairs of lines, one (SiTmp1A and SiTmp1B) for the upper modules (1, 3 and 5) and one (SiTmp2A and SiTmp2B) for the lower modules (2, 4 and 6). One thermistor only can be connected for to each line, or up to all the thermistors housed in the detectors that lie on the corresponding side of the ROD. The two temperature line pairs go out from the ICB through the HV connector housed in the HVRAC and end to two twisted pairs in the multi-service cable.

There are two additional temperature line pairs in the ROD IC bus which serve two probes (UniCurve thermistors) sitting on the ROD. One of them measures the ambient temperature (AirTmpA and AirTmpB) while the other is attached to the cooling pipe and measures the coolant temperature (LiqTmpA and LiqTmpB). These two temperature line pairs go out from the ICB through the LV connector housed in the LVRAC to another two twisted pairs in the multiservice cable.

In summary, there are four temperature lines for each ROD IC bus and for each multiservice cable, two of them read ROD temperatures, and two of them read (a combination of) silicon detector temperatures. These four lines are also available in the CCUM. One out of the two Silicon temperatures, and one out of the two ROD temperatures can be driven and readout by the DCU sitting on the CCUM rather than remotely through the multiservice cable.

Finally the connections (ITHij+, ITHij-) between the connector from/to the Front-end hybrid and the connector from/to the Kapton HV Bias PCB that are used to connect the DCU housed in the front-end hybrid to the two remaining thermistors (driven in parallel) housed in the Kapton HV Bias PCB are checked.

4.2.1. Test Setup and Hardware Equipment

The setup for the electrical test is based on a commercial DAQ PCI board (National Instruments NI6025E) with:

- 32 digital I/O channels (DIO<7:0>, PA<7:0>, PB<7:0>, PC<7:0>).
- 16 Analog Inputs (ACH<15:0>).
- 2 Analog Outputs (DACOUT<1:0>).

on a Visual Basic Interface and on a set of simple adapter cards that let to access the device under test (DUT):

- **TSMC**: Test Setup Master Card, which distributes digital and analog signals from the NI6025E board to the Device Under Test (DUT) and collects analog and digital signals from the DUT and sends them to the NI6025E board.
- **LVRAC**: Low Voltage ROD Adapter Card.
- **HVRAC**: High Voltage ROD Adapter Card
- **LVTC**: Low Voltage Test Card, which interfaces the LVRAC.
- **HVAC**: High Voltage Adapter Card, which interfaces the HVRAC.
- **DCTC**: Dummy CCU Test Card, which replaces the CCUM module during the electrical tests.
4.2.2. Test Procedures

The electrical test follows eight steps. During the first 4 steps (TESTA, TESTB, TESTC and TESTD) the ROD is not powered and the setup interfaces the DUT through LVTC, HVTC and DCTC. During the remaining 4 steps (TESTE, TESTF, TESTG and TESTH) the ROD is powered (LVTC is removed) and the dummy detector test cards (DDTC) and a front-end hybrids are plugged in all the possible 12 (6 in the SS RODs) following locations (see Figure x):

1) DDTC in MODULE 1 / DETECTOR 1 (connector HV1 in ICC1)
   HYBRID in MODULE 1 / HYBRID 1 (connector FE1 in ICC1)
2) DDTC in MODULE 1 / DETECTOR 2 (connector HV2 in ICC 1)
   HYBRID in MODULE 1 / HYBRID 2 (connector FE2 in ICC 1) – for DS RODs only
3) DDTC in MODULE 2 / DETECTOR 1 (connector HV1 in ICC 2)
   HYBRID in MODULE 2 / HYBRID 1 (connector FE1 in ICC 2)
4) DDTC in MODULE 2 / DETECTOR 2 (connector HV2 in ICC 2)
   HYBRID in MODULE 2 / HYBRID 2 (connector FE2 in ICC 2) – for DS RODs only
5) DDTC in MODULE 3 / DETECTOR 1 (connector HV1 in ICC 3/5)
   HYBRID in MODULE 3 / HYBRID 1 (connector FE1 in ICC 3/5)
6) DDTC in MODULE 3 / DETECTOR 2 (connector HV2 in ICC 3/5)
   HYBRID in MODULE 3 / HYBRID 2 (connector FE2 in ICC 3/5) – for DS RODs only
7) DDTC in MODULE 5 / DETECTOR 1 (connector HV3 in ICC 3/5)
   HYBRID in MODULE 5 / HYBRID 1 (connector FE3 in ICC 3/5)
8) DDTC in MODULE 5 / DETECTOR 2 (connector HV4 in ICC 3/5)
   HYBRID in MODULE 5 / HYBRID 2 (connector FE4 in ICC 3/5) – for DS RODs only
9) DDTC in MODULE 4 / DETECTOR 1 (connector HV1 in ICC 4/6)
   HYBRID in MODULE 4 / HYBRID 1 (connector FE1 in ICC 4/6)
10) DDTC in MODULE 4 / DETECTOR 2 (connector HV2 in ICC 4/6)
    HYBRID in MODULE 4 / HYBRID 2 (connector FE2 in ICC 4/6) – for DS RODs only,
11) DDTC in MODULE 6 / DETECTOR 3 (connector HV3 in ICC 4/6)
    HYBRID in MODULE 6 / HYBRID 1 (connector FE3 in ICC 4/6)
12) DDTC in MODULE 6 / DETECTOR 4 (connector HV4 in ICC 4/6)
    HYBRID in MODULE 6 / HYBRID 2 (connector FE4 in ICC 4/6) – for DS RODs only.

The eight steps are here described in detail. All the checks performed in each step of the electrical test and all the possible failure conditions are reported.
TESTA (LIQTMPA, LIQTMPB, AIRTMPA, AIRTMPB)

LVTC, HVTC and DCTC plugged on
ROD not powered - See Figure 14

1) Vin = 5V is applied through one Ra = 15Kohm resistor (Ra+ to PB<0>, Ra- to ACH<8> and to LIQTMPA output in TSMB) to the LIQTMPA input of LVRAC (through LVTC); the LIQTMPB input of LVRAC is connected to GND (in LVTC).

a) ACH<8> = 5V ⇒ LVRAC/ICB (LIQTMPA) + LVRAC/ICB (LIQTMPB) FAILED
b) ACH<8> = 2V ⇒ LVRAC/ICB (LIQTMPA) • LVRAC/ICB (LIQTMPB) PASSED, ICB/CCUM (LIQTMPA) + ICB/CCUM (LIQTMPB) FAILED + thermistor not connected to DCU in CCUM
c) ACH<8> = 1.25V ⇒ LVRAC/ICB (LIQTMPA) • LVRAC/ICB (LIQTMPB) PASSED • ICB/CCUM (LIQTMPA) • ICB/CCUM (LIQTMPB) PASSED • thermistor connected to DCU in CCUM

2) Vin = 5V is applied through one Rb=15Kohm resistor (Rb+ to PB<1>, Rb- to ACH<9> and to AIRTMPA output in TSMB) to the AIRTMPA input of LVRAC (through LVTC); the AIRTMPB input of the LVRAC is connected to GND (in LVTC)

a) ACH<9> = 5V ⇒ LVRAC/ICB (AIRTMPA) + LVRAC/ICB (AIRTMPB) FAILED
b) ACH<9> = 2V ⇒ LVRAC/ICB (AIRTMPA) • LVRAC/ICB (AIRTMPB) PASSED, ICB/CCUM (AIRTMPA) + ICB/CCUM (AIRTMPB) FAILED + thermistor not connected to DCU in CCUM
c) ACH<9> = 1.25V ⇒ LVLAC/ICB (AIRTMPA) • LVLAC/ICB (AIRTMPB) PASSED • ICB/CCUM (AIRTMPA) • ICB/CCUM (AIRTMPB) PASSED • thermistor connected to DCU in CCUM

TESTB (MS250, MS125, GND)

LVTC, HVTC and DCTC plugged on
ROD not powered - See Figure 15

1) Vin = 5V is applied through one Rc1/Rc2 voltage divider (Rc1 = 10Kohm, Rc2 = 10Kohm) (Rc1+ to PB<2>, Rc1-/Rc2+ to ACH<10> and Rc2- to MS250 output in TSMB) to the MS250 input of LVRAC (through LVTC); the loop is closed through the GND connection between ICB and LVTC.

a) ACH<10> = 5V ⇒ LVRAC/ICB (MS250) + LVRAC/ICB (GND) FAILED
b) ACH<10> = 2.5V ⇒ LVRAC/ICB (MS250) • LVRAC/ICB (GND) PASSED
2) Vin = 5V is applied through one Rd1/Rd2 voltage divider (Rd1 = 10Kohm, Rd2 = 10Kohm) (Rd1+ to PB<3>, Rd1-/Rd2+ to ACH<11> and Rd2- to MS250 output in TSMB) to the MS250 input of LVRAC (through LVTC); the loop is closed through the GND connection between ICB and LVTC.

\[
\begin{align*}
a) & \text{ACH}<11> = 5V \implies \text{LVRAC/ICB (MS125) + LVRAC/ICB (GND) FAILED} \\
b) & \text{ACH}<11> = 2.5V \implies \text{LVRAC/ICB (MS125) • LVRAC/ICB (GND) PASSED}
\end{align*}
\]

**TEXTC (V250, PS250, V125, PS125)**

*LVTC, HVTC and DCTC plugged on  
ROD not powered - See Figure 16*

1) Vin = V0/V1 (output V250 of TSMB connected to DACOUT<0>, V0 and V1 are two possible values for DACOUT<0>) is applied to the V250 input of LVRAC (through LVTC); the PS250 output of LVRAC is connected to ACH<12>:

\[
\begin{align*}
a) & \text{ACH}<12> \neq V0/V1 \implies \text{LVRAC/ICB (V250) + LVRAC/ICB (PS250) FAILED} \\
b) & \text{ACH}<12> = V0/V1 \implies \text{LVRAC/ICB (V250) • LVRAC/ICB (PS250) PASSED}
\end{align*}
\]

2) Vin = V0/V1 (output V125 of TSMB connected to DACOUT<1>, V0 and V1 are two possible values for DACOUT<1>) is applied to the V125 input of LVRAC (through LVTC); the PS125 output of LVRAC is connected to ACH<13>:

\[
\begin{align*}
a) & \text{ACH}<13> \neq V0/V1 \implies \text{LVRAC/ICB (V125) + LVRAC/ICB (PS125) FAILED} \\
b) & \text{ACH}<13> = V0/V1 \implies \text{LVRAC/ICB (V125) • LVRAC/ICB (PS125) PASSED}
\end{align*}
\]

**TESTD (V250lad, V125lad)**

*LVTC, HVTC and DCTC plugged on  
ROD not powered - See Figure 17*

1) Vin = V0/V1 (output V250 of TSMB connected to DACOUT<0>, V0 and V1 are two possible values for DACOUT<0>) is applied to the V250 input of LVRAC (through LVTC); the V250lad input of CCUM is connected to ACH<14> (through DCTC):

\[
\begin{align*}
a) & \text{ACH}<14> \neq V0/V1 \implies \text{LVRAC/ICB (V250) + ICB/CCUM (V250lad) FAILED} \\
b) & \text{ACH}<14> = V0/V1 \implies \text{LVRAC/ICB (V250) • ICB/CCUM (V250lad) PASSED}
\end{align*}
\]
2) $V_{in} = \frac{V_0}{V_1}$ (output V125 of MTBC connected to DACOUT<1>, $V_0$ and $V_1$ are two possible values for DACOUT<1>) is applied to the V125 input of LVRAC (through LVTC); the V125lad input of CCUM is connected to ACH<15> (through DCTC):

   a) $ACH<15> \neq \frac{V_0}{V_1} \Rightarrow LVRAC/ICB (V125) + ICB/CCUM (V125lad) FAILED$
   
   b) $ACH<15> = \frac{V_0}{V_1} \Rightarrow LVRAC/ICB (V125) \bullet ICB/CCUM (V125lad) PASSED$

**TESTE (HVij, BCKPLS1, BCKPLS2, GND)**

$HVTC$ and $DCTC$ plugged on

$DDTCij$ on $HV(Mi/Dj)$, $Hybridij$ on $FE(Mi/Dj)$, $HV$ to $DDTCij$

$ROD$ powered through $LVCAC$ - See Figure 18 and Figure 19

1) $V_{in} = 5V$ is applied through one Re1/Re2 voltage divider ($Re1 = 10Kohm$, $Re2 = 10Kohm$) ($Re1+$ to PA<0>, $Re1-/Re2+$ to BCKPLS1 and $Re2-$ to GND in TSMB) to the BCKPLS1 input of ICB (through DCTC); the BCKPLS1 signal goes to HVTC and then to $ACH<i-1>$ ($i = 1,3,5$) in TSMB through ICB, ICC I ($i = 1,3,5$), DDTC J ($J = 1,2$), high voltage wire HVi ($i = 1,3,5$, $j = 1,2$) and HVRAC:

   a) $ACH<i-1> \neq 3.3V \Rightarrow CCUM/ICB (BCKPLS1) + CCUM/ICB (GND) + ICB/ICCI (BCKPLS) + ICB/ICCI (GND) + ICCI/DETJ (BCKPLS) + ICCI/DETJ (GND) + ICB/DET (HVj) FAILED$
   
   b) $ACH<i-1> = 3.3V \Rightarrow CCUM/ICB (BCKPLS1) \bullet CCUM/ICB (GND) \bullet ICB/ICCI (BCKPLS) \bullet ICB/ICCI (GND) \bullet ICCI/DETJ (BCKPLS) \bullet ICCI/DETJ (GND) \bullet ICB/DET (HVj) PASSED$

2) $V_{in} = 5V$ is applied through one Rf1/Rf2 voltage divider ($Rf1 = 10Kohm$, $Rf2=10Kohm$) ($Rf1+$ to PA<1>, $Rf1-/Rf2+$ to BCKPLS2 and $Rf2-$ to GND in TSMB) to the BCKPLS2 input of ICB (through DCTC); the BCKPLS2 signal goes to HVTC and then to $ACH<i-1>$ ($i = 2,4,6$) in TSMB through ICB, ICC I ($i = 2,4,6$), DDTC J ($J = 1,2$), high voltage wire HVi ($i = 2,4,6$) and HVRAC:

   a) $ACH<i-1> \neq 3.3V \Rightarrow CCUM/ICB (BCKPLS2) + CCUM/ICB (GND) + ICB/ICCI (BCKPLS) + ICB/ICCI (GND) + ICCI/DETJ (BCKPLS) + ICCI/DETJ (GND) + ICB/DET (HVj) FAILED$
   
   b) $ACH<i-1> = 3.3V \Rightarrow CCUM/ICB (BCKPLS2) \bullet CCUM/ICB (GND) \bullet ICB/ICCI (BCKPLS2) \bullet ICB/ICCI (GND) \bullet ICCI/DETJ (BCKPLS) \bullet ICCI/DETJ (GND) \bullet ICB/DET (HVj) FAILED$
**TESTF (I2Cij)**

*HVTC and DCTC plugged on*
*DDTCij on HV(Mi/Dj), HYBRIDij on FE(Mi/Dj), HVi to DDTCi1*
*ROD powered through LVCAC - See Figure 20*

1) WRITE DATA_IN into DCUij_TREG, READ DATA_OUT from DCUij_TREG

a) DATA_OUT ≠ DATA_IN ⇒ CCUM/ICB (I2Cij) + ICB/ICCi (I2Cij) + ICCi/HYBij (I2Cij)
   FAILED

b) DATA_OUT = DATA_IN ⇒ CCUM/ICB (I2Cij) • ICB/ICCi (I2Cij) • ICCi/HYBij (I2Cij)
   PASSED

**TESTG (RSTi)**

*HVTC and DCTC plugged on*
*DDTCij on HV(Mi/Dj), HYBRIDij on FE(Mi/Dj), HVi to DDTC*
*ROD powered through LVCAC - See Figure Etest6*

1) WRITE DATA_IN = 0xff into DCUij_TREG, RESET MODULE I, READ DATA_OUT from DCUij_TREG

a) DATA_OUT ≠ 0x00 ⇒ CCUM/ICB (RSTi) + ICB/ICCi (RSTi) + ICCi/HYBij (RSTi)
   FAILED

b) DATA_OUT = 0x00 ⇒ CCUM/ICB (RSTi) • ICB/ICCi (RSTi) • ICCi/HYBij (RSTi)
   PASSED

**TESTH (CLK, ITH+, ITH-, SI1TMP, SI2TMP)**

*HVTC and DCTC plugged on*
*DDTCij on HV(Mi/Dj), HYBRIDij on FE(Mi/Dj), HVi to DDTC*
*ROD powered through LVCAC - See Figure Etest6*

1) ACQUIRE DCUij channel 0 → Vout

a) Vout = 1V ⇒ CCUM/ICB (CLK) • ICB/ICCi (CLK) • ICCi/HYBij (CLK) •
   HYBij/ICCi (ITH+, ITH-) • ICCi/DETij (ITH+/ITH-) PASSED,
   DETij/ICCi (SITMPA,SITMPB) + ICCi/ICB (SITMPA,SITMPB) +
   ICB/HVRA (SITMPA,SITMPB) + ICB/CCUM (SITMPA,SITMPB)
   FAILED + thermistor not connected to CCUM

b) Vout = 0.5V ⇒ CCUM/ICB (CLK) • ICB/ICCi (CLK) • ICCi/HYBij (CLK) •+
   HYBij/ICCi (ITH+, ITH-) • ICCi/DETij (ITH+/ITH-) •
   DETij/ICCi(SITMPA,SITMPB) • ICCi/ICB (SITMPA,SITMPB) •
   PASSED
ICB/HVRAC (SITMPA,SITMPB) PASSED, ICB/CCUM (SITMPA,SITMPB) FAILED + thermistor not connected to CCUM

c) $V_{out} = 0.25V$  \[\Rightarrow\] CCUM/ICB (CLK) • ICB/ICCi (CLK) • ICCi/HYBij (CLK) •+ HYBij/ICCi (ITH+,ITH-) • ICCi/DETij (ITH+/ITH-) • DETij/ICCi(SITMPA,SITMPB) • ICCi/ICB (SITMPA,SITMPB) • ICB/HVRAC (SITMPA,SITMPB) • ICB/CCUM (SITMPA,SITMPB) PASSED • thermistor connected to CCUM

5. Functionality Tests
The goal of the functionality tests is to assure a correct functioning of the cabled ROD as a complete single readout element. The functionality tests aim to test the two layers of the communication architecture proposed to control the embedded electronics of the RODs:

1. The first layer (called ring or control loop) links the FEC and CCUMs (or RODs). Optical links are used to transmit data between the back-end (FEC) and the front-end digital optohybrid (DOH). The data is then transmitted between CCUMs via electrical interconnections.

2. The second layer of communication, between the CCUM and the front-end chips is entirely electrical and it is based on the I2C standard protocol. The ROD is thus operated in a DAQ setup and exercised with internal triggers and clocks.

During the tests of cabled RODs at CERN no silicon detector modules will be inserted on the RODs. Instead, for the functionality tests, we envision to use fully functional APV hybrids connected to the interconnect cards of the ROD. To test the basic operation of the ROD bus and its connections, the APV hybrid and analogue opto-hybrid IC registers will be addressed through the I2C interface. To test the optical fiber connectivity, the APVs will be clocked and exercised with full readout cycles.

5.1. Test Setup and Hardware Equipment
The cable ROD test setup used for functionality tests consists of:

- 1 single PC computer running Linux.
- 1 trigger sequencer card (TSC).
- 1 PMC-FEC card.
- 1 FEC2CCUM interface card.
- 1 PMC-FED card.
- 2 Opto-Electrical Converter (OEC) Card (12 inputs each).
- 1 MUX motherboard.
- 3 MUX cards.
- 12 APV hybrids (6 of type up and 6 of type down).
- 250 APV hybrid adapter card connectors.

The PMC-FEC card (called electrical FEC) [2] is limited to two input and two output data lines (ports A and B) but to a single differential clock line. In order to test the redundancy functionality of the control ring architecture of the CCUMs (and RODs), an additional FEC2CCUM interface card is
needed. The FEC2CCUM card incorporates some of the functionalities of the Digital Optohybrid Module (DOHM). It has a LVDSMUX chip which splits the output clock line coming from the FEC into two clock lines (for port A or primary loop and port B or secondary loop of the control ring). The type of input clock into the FEC is controlled by using the SEL_SER_IN and SEL_SER_OUT serial data bit lines of the FEC control register 0, used for redundancy.

The FEC2CCUM board also converts the differential reset line coming out from the FEC into single-ended needed by the CCUM. The FEC2CCUM board also includes an I2C slave chip to test the CCU I2C channel lines used to control the DOHM transmitters for either the primary or secondary loops of the control ring. Finally, the FEC2CCUM board has an input 2.5 V low voltage connector to power the CCUM modules.

The TSC card [3] sends clocks and triggers to up to four PMC-FED cards through LVDS lines, and to one PMC-FEC card through an optical connection. The PMC-FED cards [4] receive and digitize analog electrical differential signals from the APV chips. It is thus also necessary an optical to electrical converter board (OEC Opto-Electrical Converter). The PMC-FED receives up to 8 readout analog optical fibers.

There will be two different types of cabled RODs depending on the type of ICC (Interconnect Cards) they will be instrumented with:

- Single sided ICCs (only one silicon detector module will be connected)
- Double sided ICCs (two silicon detector modules connected).

After inserting the silicon detector modules on cabled RODs there will be three different types of RODs, depending on the total number of readout channels (or laser analog outputs) on each:

- L1-L2 ROD (double-sided ROD) equipped with 12 detector modules of 4 - APVs (24 laser analog outputs).
- L3-L4 ROD (single-sided ROD) equipped with 6 detector modules of 4 - APVs (12 laser analog outputs).
- L5-L6 ROD (single-sided ROD) equipped with 6 detector modules of 6 - APVs (18 laser analog outputs).

In order to readout any type of ROD with a single PMC-FED card some kind of multiplexing of the data is thus necessary. The Karlsruhe multiplexer boards (MUX boards) receive as input data up to 10 optical links. The MUX boards are housed on a motherboard with communication done through an I2C interface card also placed on the motherboard.

For the functionality tests a total of 12 APV hybrids will be needed: 6 of type up and 6 of type down. From these 12 hybrids special 6 back-to-back hybrids will be assembled for the functional tests. The typical lifetime of a hybrid connector is ~ 40 connections. In order to reduce the stress on the hybrid connectors, adapter connectors plugged on the hybrid connectors will be used instead. A total of ~ 250 adapter connector will be needed for the testing of ~ 800 cable RODs.
5.2. DAQ Software

The DAQ software used to exercise the cabled RODs during production is based on the XROD program [5]. XROD uses the same hardware and low level software libraries developed in Lyon to access the back-end drivers of the DAQ cards (TSC, PMC-FEC, and PMC-FED). XROD also uses the same software libraries to access the I2C bus and perform I2C transactions (read/write) through the different channels of the CCU.

XROD provides an intuitive and easy to use tool to debug all aspects of the ROD. The program provides a direct access to:

- The different back-end devices related to the DAQ hardware (TSC card, PMC-FEC card, and PMC-FED cards).
- The registers and channels of the CCU25 chip (also the old CCU6 chip can be addressed).
- The laser driver IC registers on the analog optohybrids (AOH) of the ROD interconnect cards.
- The registers of the different IC chips on the silicon detector module hybrids (PLL, MUX, DCU, and APV chips).

The access to all these devices is done through a single main panel interface from which the user can also start different data taking runs or scan types (see Section 3.3.3).

5.3. Test Procedures

The different steps in the functionality test procedures of cabled RODs consist on CCU functionality tests, I2C bus addressing tests, digital and readout error tests, and DAQ scans.

5.3.1. CCUM Functionality Tests

Each control loop of CCUMs (or RODs) supports a redundancy scheme based on doubling signal paths and bypassing of interconnection lines between CCUs and between the CCU and the FEC. The ring consists of two independent data paths (A and B ports), one connecting the CCU modules serially (DatA and ClkA lines) and a second redundant path which alternatively skips one CCU module in the chain (DatB and ClkB lines). The communication in normal operation occurs among all adjacent CCUM modules using the A ports. Whenever one CCUM module fails the ring is configured to skip the faulty module. This is achieved by programming the module preceding the faulty one to select the B port as its output port.

The CCUM boards can be classified according to which DOHM transmitter (TxA or TxB) they are configured to address the I2C channel 15 of the CCU. This is controlled through I2C straps placed on the CCUM board. We distinguish between three different CCUM types:

- CCUM type 0: control the DOHM transmitters of the primary loop (TxA) through appropriate straps.
- CCUM type 1: control the DOHM transmitters of the secondary loop (TxB) through appropriate straps.
- CCUM type 2: all I2C Tx-straps are disabled.

The PMC-FEC and the ROD are interfaced through the FEC2CCUM adapter card described in a previous section (see Figure 10), and whose functions are the following:
• to test all the LVDS control lines (those used for the primary and secondary loops).
• to test the reset lines.
• to test the I2C lines used to control the transmitters of the DOHM of the primary loop (the first CCUM of the control loop – CCUM type 0 - is the I2C master) and of the secondary loop (the second CCUM of the control loop – CCUM type 1 - is the I2C master). There are a total of 2 input I2C lines (I2C1IN, I2C2IN) and 2 output I2C lines (I2C1OUT, I2C2OUT) to control both the primary and secondary loops.

The test of the LVDS control lines is performed in the two following steps (in the following ROD N represents the ROD under test):

• Test #1: the LVDS control lines used for the primary loop are tested:
  o DatA and ClkA from ROD N-1 to ROD N (A inputs of the ROD under test)
  o DatA and ClkA from ROD N to ROD N+1 (A outputs of the ROD under test)

• Test #2: the following LVDS control lines used for the secondary loop are tested:
  o DatB and ClkB from ROD N-1 to ROD N (B1 inputs of the ROD under test)
  o DatB and ClkB from ROD N to ROD N+1 (B1 outputs of the ROD under test)
  o DatB and ClkB from ROD N-2 to ROD N (B2 inputs of the ROD under test)
  o DatB and ClkB from ROD N to ROD N+2 (B2 outputs of the ROD under test)

• Test #3: the test of the reset lines is performed verifying that the reset is correctly received by the CCU housed in the CCUM of the ROD under test and propagated to the next ROD of the control loop using a simple LED-based circuit in the FEC2CCUM board.

The test of the I2C lines is performed verifying that the CCU housed in the CCUM of the ROD under test can correctly write and read an I2C slave chip located in the FEC2CCUM board. This test will check the following connections:

• Test #4a (CCUM type 0, i.e., first CCUM of the control loop)
  o I2C from CCU to I2C1 (internal jumpers)
  o I2C1 from ROD N to ROD N-1 (I2C1 outputs of the ROD under test)
  o I2C2 from ROD N+1 to ROD N (I2C2 inputs of the ROD under test)
  o I2C2 from ROD N to ROD N-1 (I2C2 outputs of the ROD under test)

• Test #4b (CCUM type 1, i.e., second CCUM of the control loop)
  o I2C from CCU to I2C2 (internal jumpers)
  o I2C2 from ROD N to ROD N-1 (I2C2 outputs of the ROD under test)

• Test #4c (CCUM type 2, i.e., other CCUMs of the control loop)
  o No I2C connection from CCU to I2C1 or I2C2 (internal jumpers)

The connections that are checked during the tests described above are shown in Figure 11.
5.3.2. I2C Bus Addressing

With the I2C bus addressing tests, a basic read/write access to the IC registers of the different detector hybrid chip components of the ROD is performed. A read/write access to the laser driver IC registers of the analog optohybrids on the interconnect cards is also performed. The aim is to check the electrical functionality of the I2C bus interface and the interconnect cards of the ROD by issuing transactions on all I2C channels of the CCU25. I2C data transactions are done on a byte basis over the two wire serial interface of the ROD bus (designed to conform the I2C standard), that is, each I2C cycle addresses a single 8-bit register in the IC. For an I2C transaction to begin, first an address is sent, followed by additional parameters.

XROD provides a GUI to access and test the main registers of the different IC chips connected to the ROD. Following we summarize the basic functionality of each I2C accessible IC on the ROD modules and the available registers on each of them.

5.3.2.1. PLL Addressing

The PLL ASIC extracts the LHC clock from the encoded signal and decodes the first level trigger decision. It is also used to correct the timing of the clock and trigger signals.

The ASIC and its registers are identified by a 7 bit address [2]. The two least significant bits are used to select one of the internal registers while the five most significant bits represent the I2C address. The available registers on XROD for the functional tests used to check the PLL operation through the I2C serial interface are:

*PLL Latency (Clock Delay) Register*

The PLL ASIC contains an internal clock de-skewing mechanism that allows to phase shift the clock signal up to a maximum of 25 ns in phase steps of 1.04 ns.

*PLL L1 Delay Register*

A trigger coarse skew compensation function is also implemented on the PLL ASIC that allows to delay the L1 trigger signal up to a maximum of 15 LHC clock cycles (25 ns).

5.3.2.2. MUX Addressing

The MUX ASIC interface between the APV25 chip and the optical line driver chip, multiplexing the outputs of two APV25 chips onto a single optical line driver input.

The MUX IC conforms to the usual I2C standard [3] addressed by an 8 bit word, the first 7 bits being the IC address and the least significant bit being the read/write bit. The available register on XROD for the functional tests used to check the MUX operation through the I2C serial interface is:

*MUX Resistor Register*

The MUX chip has four channels, each consisting of a 2-to-1 multiplexer. The differential current outputs of the APV chips are converted into voltages by internal resistors. Each MUX chip consists of 8 resistors in parallel connected between each differential input and a reference voltage pad. Each resistor has a value of 400 Ohms. Switches in series with each of these enable the resistance value to
be varied between 400 Ohms and 50 Ohms. The switches are controlled by signals from an 8-bit register loaded via the chip’s I2C interface.

5.3.2.3. DCU Addressing
The DCU (Detector Control Unit) is a special ASIC used for the monitoring of some embedded parameters like supply voltages and currents on the front-end read-out modules. The access to the internal registers of the DCU is available through the I2C interface. The user can select one of the ADC input channels, start an ADC acquisition and read the ADC output simply by accessing different I2C registers.

The access to the DCU IC registers [4] follows the I2C standard protocol. The five most significant bits of the 7 bit I2C address are used to address the chip on the I2C bus. The remaining two bits are used to address the internal registers. The available registers on XROD for the functional tests used to check the DCU operation through the I2C serial interface are:

**DCU Resistor Register**
The MUX chip ha

5.3.2.4. AOH Addressing
The AOH (Analog Opto Hybrid) boards contain linear laser driver ICs and laser diodes necessary for the conversion of the analog data produced by the front-end APV chips into amplitude modulated optical signals [5]. Each AOH holds one linear laser driver IC made of three laser drivers and an I2C interface. Each driver takes a differential input voltage and converts it into an unipolar current used to modulate an external laser diode. Besides signal modulation, each driver also generates a DC current used to bias the external laser diode. This current allows the laser-diode to be operated above threshold in the linear region of its characteristics.

The linear laser driver IC implements the standard I2C protocol and it is addressed using a seven bit address number. The two less significant bits address the AOH IC internal programming registers. The five most significant bits are the AOH IC address which are configured with the external ASIC inputs. The available registers on XROD for the functional tests used to check the AOH operation through the I2C serial interface are:

**AOH Gain Register**
The linearity of the output current for each laser driver is guaranteed for input differential voltages between ±300 mV. Above ±500 mV the output current is not specified and can eventually saturate. The driver trans-conductance is pre-settable among four different values (5, 7.5, 10 and 12.5 mS) by acting on the gain registers. This results in an output current range of ±2, ±3, ±4 and ±5 mA respectively, when the input differential voltage changes from -400 mV to +400 mV. The gain programming register determines the gain of the individual channels.

**AOH Bias Register**
Ageing and performance degradation due to radiation cause the laser diode threshold currents to change with time. To compensate for these variations the laser diode bias current is made programmable through the I2C interface. As each device in the group has different thresholds and might age differently, the bias current produced by each driver is made individually programmable
through the I2C interface. There are three laser diode bias current registers. The bias current is approximately given between 0-55 mA in steps of 0.45 mA. The bias current programming registers also control the power-down function for each individual channel. When set to zero, the power-down function is activated and the driver disable. This reduces the power consumption and noise of a non-used or defective channel.

5.3.2.5. APV Addressing
The APV is a 128-channel analogue pipeline chip for the readout of the silicon detectors. Each channel comprises an amplifier, a 192-cell analogue pipeline and a deconvolution readout circuit. The output data are transmitted on a single differential current output via an analogue multiplexer.

The APV chip configuration, bias settings and error states are handled over the I2C standard interface [5]. The access to the APV registers is done through I2C transfers comprising cycles of three 8 bit data packets:

1. The chip address, given by the standard 7 bits with the most significant two bits set to “01” and the remaining five defined by bonding out the address pads of the chip.
2. The command register, which determines which of the other APV registers is to be accessed, with the direction of the data transfer.
3. The 8 bit data value.

The available registers on XROD for the functional tests used to check the APV operation through the I2C serial interface are:

**APV Mode Register**
The APV mode register is used to select the basic readout configuration of the APV: analog bias, trigger mode, readout mode, preamplifier polarity, calibration inhibit, and readout frequency.

**APV Bias Generator Register**
The APV bias generator register defines the bias settings of the chip.

**APV Latency Register**
The APV latency register is an 8 bit binary number which defines the separation between the write and trigger pointers in the pipeline memory control. Its value can be programmed to any value up to 191.

**APV MuxGain Register**
The APV muxgain register contains an 8 bit pattern which defines which size resistor to use in the input stage of the multiplexer.

**APV Calibration Control Register**
The APV calibration registers relate to the internal pulse generator. They define the timing of the test pulses (CSEL register) and the channels to which they are applied (CDRV register).
5.3.3. Digital Tests and Readout Errors

The purpose of these tests is to check all APVs can be operated and readout on a final cabled ROD. This test is more useful on final RODs (with detector modules mounted on them) although its use on cabled RODs with hybrids at CERN is recommended to assure a good performance of the cabled ROD as a whole working readout unit. A basic and fast run scan provided by the XROD DAQ software monitors the synchronicity of all chips in the readout chain and scans pipeline locations looking for bad addresses. Readout errors can be checked by parsing the APV data header. They are defined as events with at least:

- An APV error bit set to logic 0.
- A mismatch column address between APV chips.
- Bad pipeline cell locations.
- FED digitization error (FED boards out of sync, bad timings, etc.).

5.3.4. DAQ Scans

The purpose of these tests is to ch

- **Noise Scans** with real time visualization of frames, pedestals, noise, pipeline cell distributions, and an event error summary. A simple cluster algorithm is also run in real time when running the devices with external triggers, with a source profile and a cluster charge online histogram distribution.
- **Timing Scans** to find automatically the optimal timing for the test setup, i.e., the best PMC-FED clock delays (for each PMC-FED) and PLL settings.
- **Gain Scans**, to perform a quick calibration gain scan. The user defines the scan parameters (start values, end values, and steps of calibration pulse amplitudes and groups of channels to send the pulses).
- **Pulse Shape Scans**, to perform quick calibration pulse shape scans.
- **Optical Scans**, to find the best operating conditions for the analog optohybrids in terms of bias and gain settings.
- **DCU Scans**, to perform stand-alone DCU scans with a real time monitoring of silicon and brid temperatures, leakage current, and low voltages.
References


Figure A1: Cabled ROD.

Figure A2: Module numbering scheme for cabled RODs.

Figure A3: Distribution of number and types of RODs per layer for the two barrels of the TOB. Also shown are the number of control loops per layer for each half side of the TOB. DS RODs populate layers 1 and 2. Layers 3 to 6 are populated by SS RODs. DS RODs of layer 1 have the r-ϕ detectors at a lower radius while the stereo detectors are at a higher radius. The opposite situation stands for the DS RODs of layer 2.

Total RODs (Z<0): 344

Total RODs (Z>0): 344
Figure 1: Test board PCB (Test Bed Card Board) for the CCUM test setup (top) and its mechanical assembly fixture (bottom).
Figure 2: User interface program for the CCUM tests.
Figure 3: TOB ROD control input/output connectors and CCUM electrical connections to be tested.

Figure 4: V250 and ground input and output lines tests.
Figure 5: CCUM Control ring connection tests.

Figure 6: CCUM I2C lines and parallel port lines tests.
Figure 7: Reset In/Out and system clock lines tests.

Figure 8: DCU, ROD power lines and strapped sensors tests.
Figure 9: CCUM flow of tests.
Figure 10: Connections among the FEC, FEC2CCUM, and CCUM during the functional tests.
Test #1: primary loop

Test #2: secondary loop

Test #3: reset

Figure 11: Connections to/from CCUM checked during the functional test.
Figure 12: Connections to/from CCUM checked during the functional test.
Figure 13: Test setups for the electrical and for the functional test.

- 1) Electrical Test phase 1 (ROD not powered)
- 2) Electrical Test phase 2 (ROD not powered)
- 3) Functional Test

*Note: The diagram shows interconnected test setups with labels such as 2VPS, TC, and other electrical components.*
Figure 14: Connections checked during the electrical test A.
Figure 15: Connections checked during the electrical test B.
Figure 16: Connections checked during the electrical test C.
Figure 17: Connections checked during the electrical test D.
Figure 18: Connections checked during the electrical test E (Modules 1, 3 and 5).
Figure 19: Connections checked during the electrical test E (Modules 2, 4 and 6).
Figure 20: Connections checked during the electrical tests F, G and H.