CMS Internal Note

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XROD
A Program for ROD Characterization and ROD System Tests

Juan Valls
(valls@cern.ch)
CERN

Abstract
This note describes the XROD program, a fast diagnostic tool for electrical characterization of CMS silicon detector modules and TOB ROD devices. Both the program and the GUI interface have been written in C and C++. XROD allows to write/read the IC chip registers of the silicon module hybrid front-end boards as well as the laser drivers IC registers of the analogue opto-hybrids boards. It is also possible, and from the same interface, to access the register settings of the back-end DAQ boards (TSC, FEC, CCU, and FED). XROD visualizes in real time noise and pedestal scans, calibration test pulse (gain) scans, FED timing and alignment scans, calibration test pulse shape scans, optical characterization of analogue links (bias and
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1 Introduction

XROD provides an intuitive and easy to use tool to debug all aspects of the ROD. XROD can be used to readout from a single detector silicon module (with either 4 or 6 chips) to several RODs simultaneously. Data can be logged in either ASCII files or ROOT files format.

XROD uses the same hardware and low level software libraries developed in the framework of the so called CMS-like DAQ software to access the back-end drivers of the CMS tracker DAQ cards (TSC, PMC-FEC, CCU, and PMC-FED). XROD also uses the same software libraries from the CMS-like software to access (read/write) the I2C bus channels and parallel PIO port channels of the CCU. XROD is designed to be more a system test tool than a data acquisition software optimized for long burn-in runs. XROD can, though, still take data and log it on disk with either internal or external (β-source, cosmics) triggers.

The XROD software is being used at the system test setups of the first single sided and double sided prototype RODs in Building 598 at CERN. It will be used during the functionality tests of electrical cabled RODs at CERN [1] as well as for quick characterization tests of full RODs (with silicon) at USA and at CERN during production [2].

2 Installation and Setup

The last version of the XROD program as well as related libraries can always be found to download at the following URL address: http://cern.ch/valls/xrod.htm.

To install the program download the latest version and follow these steps:

- Select a directory where to install XROD, i.e., $HOME/xrod_vxx (where xx is the XROD version number).
- Unzip the tar archive with (xx stands for the XROD version number):
  
gunzip xrod_vxx.tar.gz
- Unpack the tar archive in the directory where you want the program to be installed:
  
tar xvf xrod_vxx.tar
- Edit the Makefile in the src directory to fit your platform needs.
- Type:
  
  make clean followed by make

Define the environmental variable XROD_HOME to point to the main directory where XROD is installed, i.e.:
In order to run XROD from any directory it is advisable to create a simple script like:

```bash
#!/bin/bash
cd $HOME/xrod_vxx/src
./xrod
```

and place it in the home directory.

After these steps one can start XROD from any directory. Figure 1 shows a picture of the XROD Main Menu window. Select from the File menu in the menu bar the Set Options menu. The XROD Configuration window shown in Figure 2 will show up. From this menu the user defines default values used in XROD each time it starts. The different settings accessible from the XROD Configuration window are:

1. The default print command and data path directory (where the data will be stored) assigned everytime XROD is launched.

2. XROD works with configuration files which specify the number of devices under control of XROD and their hardware addresses. The configuration files also define default values of the registers for the different front-end chips. Figure 3 shows an example of a configuration file for one silicon detector module with 4 APVs. The default configuration file loaded everytime XROD is launched is selected also from the XROD Configuration window (Set Initial Device) from a list of 5 possible options:
   - 1 silicon detector module with 4 APVs.
   - 1 silicon detector module with 6 APVs.
   - 1 SS (Single Sided) ROD with 6 silicon detector modules of 4 APVs each.
   - 1 SS ROD with 6 silicon detector modules of 6 APVs each.
   - 1 DS (Double Sided) ROD with 12 silicon detector modules of 4 APVs each.

3. The user can also set the initial (or default) mode of hardware access everytime XROD is launched in the XROD Configuration window. If set to TRUE, every time XROD starts it will try to access the default hardware. If the hardware is turned off (no low voltage applied to the devices) or the hardware addresses are not set correctly, the program will fail and an error message will be issued. It is recommended to set the default hardware access to FALSE.

At the top of the XROD Main Menu window the loaded configuration file is always displayed (see Figure 1). From the Select Modules or Select RODs menus in the menu bar the user can select a different configuration file corresponding to the following options:

- **Select Modules:**
  - 1 Module (4 APVs).
  - 1 Module (6 APVs).
Select Combination of Modules (Figure 4).

- Select ROD:
  - 1 SS ROD (24 APVs).
  - 1 SS ROD (36 APVs).
  - 1 DS ROD (48 APVs).

Select Combination of RODs (Figure 4).

From the Select Combination of Modules and Select Combination of RODs the user can select the number and type of silicon detector modules and ROD devices, respectively (see Figure 4).

New default values for the configuration files can always be changed at any time by:

- Editing the appropriate configuration file and changing the default values directly. The XROD configuration files are stored under the directory $HOME/xrod_vxx/conf directory. Default configuration files can always be found under the directory $HOME/xrod_vxx/conf/default_conf_files.
- Setting the new values of the different registers and hardware addresses in the different display menus and then clicking on the Save New Hardware Defaults button at the top of the main XROD window.

After selecting a particular device from the Select Modules or Select RODs menus, if the selected configuration file does not exist it will automatically be created by XROD. The user should check and overwrite its values with the appropriate ones.

XROD handles up to 3 PMC-FED cards without the MUX hardware. This means the readout of any of the following devices:

- Up to 8 silicon detector modules of any APV chip multiplicity (4 or 6 APVs).
- 1 SS ROD with 6 silicon detector modules of any APV multiplicity (4 or 6 APVs).
- 1 DS ROD with 12 silicon detector modules (4 APVs each).
- Up to 2 SS RODs with 6 silicon detector modules of 4 APVs each.

The Access Hardware display button indicates whether XROD is ready to access any DAQ device or front-end chip. If it is red there is no hardware access. To get ready to access the hardware click on it and it will become green if no hardware access error occurs. With the Access Hardware button XROD basically enables the I2C and PIO channels of the CCU and initializes the selected number of I2C channels.

3 Using XROD

XROD allows the user to have access to:
• The different back-end boards and registers related to the DAQ hardware (TSC card, PMC-FEC card, CCUM modules, and PMC-FED cards).
• The laser driver IC registers on the analog optohybrids (AOH front-end chips).
• The registers of the different front-end IC chips on the silicon detector module hybrids (PLL, MUX, DCU, and APV chips).

The access to all these devices and registers is done through a single main panel interface from which the user can also start different data taking runs or scan types described in next sections.

3.1 The Main Menu

From the Main Menu (Figure 1) one can kill all DAQ processes and clear semaphores and share memory resources pending from previous CMS-like DAQ related processes.

3.2 The TSC Menu

From the TSC Menu (Figure 5) the user has access to the different TSC (Trigger Sequencer Card) registers which allow to set the clock and trigger conditions. The sequencer part of the TSC matches all APV requests including trigger, calibration and reset [3].

The TSC board is presented in a PCI format and it is placed between the trigger and clock source and the FEC-CCU. At present, the TSC is usually used with an internal 40 MHz clock generator although it also may accept an ECL external clock. An optical output connects to the optical FEC input. One TSC board feeds with clocks and triggers up to 4 PMC-FED boards.

XROD only handles one TSC card. The selected TSC device number is shown at the top of the TSC Menu window. It can be changed to a new value or restored to the default one with the Set and Set Default Device buttons, respectively. The available registers on XROD to set the TSC settings are given by (Figure 5):

3.2.1 TSC Trigger Control Register

The Trigger Control Register handles the trigger source (no trigger, internal, external or soft), the inhibit trigger status bit (on/off), the interrupt trigger status bit (on/off), the calibration status bit (on/off), the reset status bit (on/off), and the clock source (internal/external).
3.2.2 TSC Trigger Mode Registers

The Trigger Mode Register controls the internal trigger frequency settings (in steps of 25 µs), the minimum number of clocks between triggers (for external triggers only, between 3 and 65535), and the maximum trigger count (if set to zero, continuous internal triggers are produced). The trigger counter read-only register can also be monitored. Finally a re-enable trigger (reset trigger filter) and a soft trigger request can also be sent through the Write Reset Trigger Filter and Write Send Soft Reset buttons, respectively.

3.2.3 TSC Trigger Gate and Encoder Registers

A set of trigger gate registers DLLs provide a local gate signal synchronized with the 40 MHz clock programmable in position and width in steps of 1 ns (from 0 to 24). If the external trigger rising edge happens during the high level of this gate the trigger is accepted and a signal output trigger (of 25 ns duration) is generated in the following clock period.

At present, the TSC trigger gate position user delay and width user value registers are not functioning within XROD and the user has to run special software to control them if external trigger operation is required with the TSC.

The TSC encoder is used to receive the APV clock and trigger outputs of the sequencer in order to encode them and supply the encoded signal to the FEC. Sometimes it has to be reset by writing the Send Reset Encoder PLL button.

3.2.4 TSC APV Sequencer Registers

With the TSC APV sequencer register the user can set the APV, calibration, and reset latencies (in clock units). These latencies are defined as the difference in time between the trigger input of the sequencer and the output sequence, which can be:

- A trigger to the APV.
- A calibration sequence (110 sequence).
- A reset sequence to the APV (101 sequence).

A reset sequence (101 sequence) can also be sent at any time through the Send APV Soft Reset write button.

3.2.5 TSC FED Sequencer Registers

The TSC can drive up to 4 FED clock and triggers via the front panel connector. The TSC FED sequencer registers accessed from XROD are:

- The TSC FED latency, which is the difference between the trigger input to the TSC sequencer and the FED trigger output. It is given in clock units and usually used to handle the FED without header finding (Scope Mode, see the FED Menu in Section 3.10.2).
- The TSC FED clock delay, fine tunable in steps of 1 ns (from 0 to 24 ns).
- The TSC FED trigger delay, also fine tunable in steps of 1 ns (from 0 to 24 ns).

In order to reset the FED trigger counter, a reset sequence 101 can also be sent through the *Send FED Soft Reset* write button (at the same time, an APV soft trigger reset is also sent).

All delay lines mentioned above are set to zero by the TSC FPGA at power on. The user can write/read all TSC registers by clicking on the *Write All/Read All* buttons at the bottom of the screen, respectively. The *Set Default* button will set default values for all registers.

### 3.3 The FEC Menu

From the *FEC Menu* (Figure 6) the user has access to different PMC-FEC card registers. The FEC (Front End Control) module [4] is implemented as a PMC module, i.e., a board with a PCI interface. The FEC is part of the slow control ring architecture of the CMS tracker. The first component of this ring is the FEC, which controls the ring, then the optical drivers and receivers that bring the clock and data to the CCU (DOH, Digital Opto Hybrid), and finally to the CCUs. The CCU (Communication and Control Unit) [5] contains the I2C masters that interface to the front-end electronics (the DCU, the APV, the MUX, and the PLL chips). The ring continues through several CCUs until the data is returned to the FEC where the status of an operation is returned. CCUs are typically mounted on Control Modules (CCUM), housing the necessary ancillary electronics, such as line drivers, receivers and level translators (see Section 3.4).

XROD only handles 1 FEC board. The selected FEC device number is shown at the top of the *FEC Menu* window. It can be changed to a new value or restored to the default one with the *Set* and *Set Default Device* buttons, respectively.

The available registers on XROD to handle the FEC are the following (Figure 6):

#### 3.3.1 Send TTCRX Init

The FEC has a TTCRx module with its associated fiberoptic receiver. The TTCRx is used to generate the clock for the CCU token ring as well as to insert the trigger information received from the TSC on the fiber. The default configuration for the TTCRx operation mode is stored in a serial EEPROM loaded into the TTCRx upon power up or when a reset is generated in the FEC.

With the *Send TTCRX Init* button the user asks to initialize the TTCRx.
3.3.2 Send Hard Reset

The FEC has a PLX PCI 9080 chip which interfaces the host PCI bus (PMC module) and the local PC bus. The different configuration of the internal registers of the PCI 9080 are stored in a serial EEPROM.

With the Send Hard Reset button a reset signal is sent to the FEC driver, the FEC PLX chip is re-initialized and the driver internals are also re-initialized. Note that the TTCRx is not re-initialized by the driver. To do so, the user must send a Send TTCRX Init after reset.

3.3.3 Send Soft Reset

With the Send Soft Reset button a reset signal is sent to the FEC driver, the FEC is re-initialized but the driver stays in its current state.

3.4 The CCU Menu

From the CCU Menu (Figure 7) the user has access to different CCUM channels (and registers) in the system. The CCU IC placed in the CCUM is described in [5].

XROD handles two different type of CCU chips: the old CCU6 and the new CCU25 chips. The CCU6 handles up to 10 I2C CCU channels (addresses 0x01-0x10). The CCU25 handles up to 16 I2C CCU channels (addresses 0x10 to 0x1F). The CCU6 has only 2 PIO parallel ports (handled with a single CCU channel with address 0x12) while the CCU25 incorporates 4 PIO ports (4 CCU channels with addresses 0x30-0x33). These PIO channels are used to send global reset lines as well as back-plane pulses to the silicon detector modules attached to the CCU.

The CCU address (in decimal) is set at the top of the CCU Menu. With the Set Address and Set Default Addresses (All CCUs) the user can set new CCU addresses or restore default ones, respectively, for the selected CCU.

The user can set the type of the CCU chip (CCU6 or CCU25) with the Select CCU IC Type radio button in the CCU Menu. In the configuration files, CCU type 0 corresponds to CCU6 and CCU type 1 corresponds to CCU25.

The available commands and registers in XROD to handle the CCU are given by:

3.4.1 Reset Lines and Back-Plane Pulse Signals

The ROD has 6 available reset lines and 2 back-plane pulse lines in its bus. These 8 lines are addressed by the PIO port A channel of the CCU25. The user can issue individual or combined reset and back-plane pulse signals to the ROD through this menu.
3.4.2 PIO parallel port registers

The user can write/read the different registers to control the 4 PIO ports of the CCU25. These ports are usually referred to as Port A, B, C, and D. Each port has 4 different registers: GCR (General Control Register), SR (Status Register), DDR (Data Direction Register), and DREG (Data REGISTER).

3.5 The PLL Menu

From the PLL Menu (Figure 8) the user has access to the different PLL IC registers of the detector hybrids. The PLL (Phase Locked Loop) ASIC extracts the LHC clock from the encoded signal coming from the CCU and decodes the first level trigger decision. It is also used to correct the timing of the clock and trigger signals when large detector multiplicity devices are readout simultaneously [6].

The CCU address (in decimal) and I2C channel number of the CCU associated with the selected PLL (also in decimal) are set at the top of the PLL Menu.

I2C data transactions to and from the PLL ASICs are done on a byte basis (each I2C cycle addresses a single 8-bit register in the IC). The PLL ASIC and its registers are identified by a 7-bit address (the 7 MSB of the 8-bit I2C address). The two least significant bits are used to select one of the internal registers while the five most significant bits represent the I2C hardware address. The PLL I2C hardware address is also set at the top of the PLL Menu (in decimal).

With the Set Channel button the user can set new values for the PLL chip I2C hardware address, CCU address and I2C channel for the selected PLL. With the Set Default Channels (All PLLs) button the user restores the default values for the PLL I2C hardware addresses, CCU addresses and I2C channels for all PLLs in the system.

The available registers on XROD to set the PLL settings through the I2C serial interface are given by (Figure 8):

3.5.1 The PLL Latency

The PLL ASIC contains an internal clock de-skewing mechanism that allows to phase shift the PLL clock signal coming from the CCU from 0 to 25 ns in phase steps of 1.04 ns. The values of the Phase and PhaseInvert register bits which control the phase shift of the clock [6] are also shown in the PLL Menu.

3.5.2 The PLL L1 Delay

A trigger coarse skew compensation function is also implemented on the PLL ASIC that allows to delay the L1 trigger signal coming from the CCU up to a maximum of 15 LHC clock cycles (4 bits value, from 0 to 15 [6]).
The user can set the PLL registers for the selected PLL by clicking on the Set button at the bottom of the screen. The settings for the selected PLL can be applied to all PLL’s by clicking on the Set All PLLs button. The Set Defaults (All PLLs) button sets the defaults for each PLL in the system. With the PLL ← and PLL → buttons one can visualize the settings for each PLL defined in the system.

### 3.5.3 Init PLL

With the Init PLL button the user can reset the PLL ASIC via the I2C interface.

### 3.6 The MUX Menu

From the MUX Menu the user has access to the MUX IC registers (Figure 9). The MUX ASIC interface between the APV25 chip and the optical line driver chip, multiplexing the outputs of two APV25 chips onto a single optical line driver input [7].

The CCU address (in decimal) and the I2C channel of the CCU associated with the selected MUX IC (also in decimal) are set at the top of the MUX Menu.

The MUX IC conforms to the usual I2C standard addressed by an 8 bit word, the first most significant 7 bits being the I2C hardware address and the least significant bit being the read/write bit. The MUX I2C hardware address associated with the selected MUX chip is also set at the top of the MUX Menu. With the Set Channel button the user can set a new value for the MUX I2C hardware address, CCU address and I2C channel associated with the selected MUX chip. With the Set Default Channels (All MUXs) button the user restores the default MUX I2C hardware addresses, CCU addresses and I2C channels for all MUXs in the system.

The available register on XROD to set the MUX settings through the I2C serial interface is (Figure 9):

### 3.6.1 The MUX Resistor

The MUX chip has four channels, each consisting of a 2-to-1 multiplexer. The differential current outputs of the APV chips are converted into voltages by internal resistors. Each MUX chip has 8 resistors in parallel connected between each differential input and a reference voltage pad. Each resistor has a value of 400 Ohms. Switches in series with each of these resistors enable the resistance value to be varied between 400 Ohms and 50 Ohms. The switches are controlled by signals from an 8-bit register loaded via the chip’s I2C interface. The number of bits ON in this register indicates the number of resistors added in parallel. The chip does not care the order the bits are turned ON, just the absolute number. The resultant termination resistance seen by each APV will then be 400 Ohm/(Nb of bits ON). XROD implements the simplest series to set these values in the configuration files:
<table>
<thead>
<tr>
<th>R (Ohms)</th>
<th>0</th>
<th>50</th>
<th>57</th>
<th>67</th>
<th>80</th>
<th>100</th>
<th>133</th>
<th>200</th>
<th>400</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value in Conf. File</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>7</td>
<td>15</td>
<td>16</td>
<td>18</td>
<td>22</td>
<td>255</td>
</tr>
</tbody>
</table>

From the MUX Menu the user has access to write/read the 9 possible values of the MUX resistor register. The resistance value to select should match the termination resistor on the analog optohybrid to get the correct signal size.

The user can set the MUX registers for the selected MUX by clicking on the Set button at the bottom of the screen. The settings for the selected MUX can be applied to all MUX’s by clicking on the Set All MUXs button. The Set Defaults (All MUXs) button sets the defaults for each MUX. With the MUX ← and MUX → buttons one can visualize the settings for each MUX.

### 3.7 The OptoHybrid Menu

From the OptoHybrid Menu the user has access to the different AOH (Analog Opto Hybrid) IC registers (Figure 10). The AOH boards contain linear laser driver ICs and laser diodes necessary for the conversion of the analog data produced by the front-end APV chips into amplitude modulated optical signals [8]. Each AOH holds one linear laser driver IC made of three laser drivers and an I2C interface. Each driver takes a differential input voltage and converts it into an unipolar current used to modulate an external laser diode. Besides signal modulation, each driver also generates a DC current used to bias the external laser diode. This current allows the laser-diode to be operated above threshold in the linear region of its characteristics.

XROD handles the two different existing AOH boards: the unpackage AOH old boards (LLD1 with four laser drivers) and the new production AOH package boards (LLD2 with three laser drivers). The user can set the type of any of the AOH boards being used with the Select Laser Driver Type radio button at the top of the OptoHybrid Menu. In the configuration files, OPTO type 0 corresponds to LLD1 optohybrids, and OPTO type 1 to LLD2 optohybrids.

The CCU address (in decimal) and I2C channel number of the CCU associated with the selected AOH board (also in decimal) are set at the top of the OptoHybrid Menu.

The linear laser driver IC implements the standard I2C protocol and it is addressed using a seven bit address number. For the old LLD1 AOH the three less significant bits address the AOH IC internal programming registers, while the four most significant bits are the AOH IC address (I2C hardware address). For the new LLD2 AOH the two less significant bits address the AOH IC internal programming registers, while the five most significant bits are the AOH IC address which are configured with the external ASIC inputs (I2C hardware address). The AOH I2C hardware address associated with the selected AOH is also set at the top of the OptoHybrid Menu. With the Set Channel button the user can set a new value for the CCU address, the I2C channel associated with the
selected AOH, and the AOH I2C hardware address. With the *Set Default Channels (All OptoHybrids)* button the user restores the default CCU addresses, I2C channels, and I2C hardware addresses for all AOHs in the system.

The AOH channel refers to the linear laser driver number. For LLD1 AOH boards, channels go from 0 to 3. Channel 0 is not connected. Channel 2 is missing for LLD1 AOH boards with only 2 instrumented laser drivers. For LLD2 AOH boards, channels go from 0 to 2. Channel 1 is missing for LLD2 AOH boards with only 2 instrumented laser drivers.

The available registers on XROD to set the AOH settings through the I2C serial interface are the following (Figure 10):

**3.7.1 AOH Gain**

The linearity of the output current for each laser driver is guaranteed for input differential voltages between ±300 mV. Above ±500 mV the output current is not specified and can eventually saturate. The driver trans-conductance is pre-settable among four different values (5, 7.5, 10 and 12.5 mS) by acting on the gain registers. This results in an output current range of ±2, ±3, ±4 and ±5 mA respectively, when the input differential voltage changes from -400 mV to +400 mV. The gain programming register determines the gain of the individual channels.

**3.7.2 AOH Bias**

Ageing and performance degradation due to radiation cause the laser diode threshold currents to change with time. To compensate for these variations the laser diode bias current is made programmable through the I2C interface. As each device in the group has different thresholds and might age differently, the bias current produced by each driver is made individually programmable through the I2C interface. There are three laser diode bias current registers. The bias current is approximately given between 0-55 mA in steps of 0.45 mA. The bias current programming registers also control the power-down function for each individual channel. When set to zero, the power-down function is activated and the driver disable. This reduces the power consumption and noise of a non-used or defective channel.

The user can set the AOH registers for the selected AOH by clicking on the *Set* button at the bottom of the screen. The settings for the selected AOH can be applied to all AOH’s by clicking on the *Set All Optohybrids* button. The *Set Defaults (All Optohybrids)* button sets the defaults for each AOH. Note that this actions DO NOT ACTUALLY write the registers on the AOHs. They only set the values on the display. To write/read the values of the registers the user should use the *Write* and *Read* buttons for each laser driver. With the *OptoHybrid ←* and *OptoHybrid →* buttons one can visualize the settings for each AOH.
3.8 The APV Menu

From the APV Menu (Figure 11) the user has access to the different APV IC registers. The APV is a 128-channel analogue pipeline chip for the readout of the silicon detectors. Each channel comprises an amplifier, a 192-cell analogue pipeline and a deconvolution readout circuit. The output data are transmitted on a single differential current output via an analogue multiplexer.

The CCU address (in decimal) and the I2C channel of the CCU associated with the selected APV (also in decimal) are set at the top of the APV Menu.

The APV chip configuration, bias settings and error states are handled over the I2C standard interface. The access to the APV registers is done through I2C transfers comprising cycles of three 8 bit data packets [9]:

1. The chip address, given by the standard 7 bits with the most significant two bits set to “01” and the remaining five defined by bonding out the address pads of the chip.
2. The command register, which determines which of the other APV registers is to be accessed, with the direction of the data transfer.
3. The 8 bit data value.

The APV I2C hardware address associated with the selected APV is also set at the top of the APV Menu. With the Set Channel button the user can set a new value for the APV I2C hardware address, CCU address and I2C channel for the selected APV. With the Set Default Channels (All APVs) button the user restores the default APV I2C hardware addresses, CCU addresses and I2C channels for all APVs in the system.

The available registers on XROD to set the APV settings through the I2C serial interface are given by (Figure 11):

3.8.1 APV Mode Register

The APV mode register is used to select the basic readout configuration of the APV: analog bias, trigger mode (1-sample/3-samples), readout mode (peak/deconvolution), preamplifier polarity (inverting/non-inverting), calibration inhibit (on/off), and readout frequency (20 MHz/40 MHz).

The trigger mode and readout mode settings combine to give the three modes of operation of the APV25 [9]:

<table>
<thead>
<tr>
<th>APV Mode</th>
<th>Trigger Mode</th>
<th>Readout Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deconvolution</td>
<td>3-samples</td>
<td>Deconvolution</td>
</tr>
<tr>
<td>Peak</td>
<td>1-sample</td>
<td>Peak</td>
</tr>
<tr>
<td>Multi</td>
<td>3-samples</td>
<td>Peak</td>
</tr>
</tbody>
</table>
3.8.2 APV Bias Generator Register

The APV bias generator register defines the bias settings of the analogue stages of the chip [9]. The bias generator requires a reference current from which all its levels are scaled. This is usually generated by reference to an internal current source designed to supply 128 µA to the bias generator.

3.8.3 APV Latency Register

The APV latency register is an 8-bit binary number which defines the separation between the write and trigger pointers in the pipeline memory control. Its value can be programmed to any value up to 191 (192 pipeline locations).

3.8.4 APV MuxGain Register

The APV muxgain register contains an 8-bit pattern which defines which size resistor to use in the input stage of the multiplexer.

3.8.5 APV Calibration Control Register

The APV calibration registers relate to the internal pulse generator. They define the timing of the test pulses (Csel register) and the channels to which they are applied (Cdrv register). The Csel register can be programmed from 0 to 7 (×3.125 ns). The Cdrv register controls 8 calibration sets of channels masked when a calibration operation is performed. Cdrv can be programmed from 0 (channels 0, 8, 16, …, 127) to 7 (channels 7, 15, 23, …, 127).

The Ical register controls the Calibrate Edge Generator Current Bias. With the internal nominal current source, Ical=29 corresponds to ~25000 electrons.

The user can set the APV registers for the selected APV by clicking on the Set button at the bottom of the screen. The settings for the selected APV can be applied to all APV’s by clicking on the Set All APVs button. The Set Defaults (All APVs) button sets the defaults for each APV. Note that these actions DO NOT ACTUALLY write the registers of the chips. They only set the values on the display. The Write All Registers and Read All Registers buttons write and read, respectively, the present register settings for the selected APV. With the APV ¯ and APV → buttons one can visualize the settings for each APV.

3.9 The DCU Menu

From the DCU Menu (Figure 12) the user has access to the different DCU IC registers. The DCU (Detector Control Unit) is a special ASIC used for the monitoring of some embedded parameters like supply voltages and currents on the front-end read-out modules. The access to the internal registers of the DCU is available through the I2C
interface. The user can select one of the ADC input channels, start an ADC acquisition and read the ADC output simply by accessing different I2C registers.

The CCU address (in decimal) and the I2C channel of the CCU associated with the selected DCU (also in decimal) are set at the top of the DCU Menu.

XROD handles two different existing DCU chips: the old DCU1 chips and the new production DCU2 chips. The user can set the type of any of the DCU chips being used with the Select DCU radio button at the top of the DCU Menu. In the configuration files, DCU type 1 corresponds to the DCU1 chips, while DCU type 2 corresponds to the DCU2 chips.

The access to the DCU IC registers follows the I2C standard protocol [10]. For the DCU2 chips, the five most significant bits of the 7-bit I2C address are used to address the chip on the I2C bus. The remaining two bits are used to address the internal registers. For the DCU1 chips, the 4 MSBs of the 7-bit I2C address are used to address the chip on the I2C bus, and the remaining 3 bits are used to address the four internal registers. The DCU I2C hardware address associated with the selected DCU is also set at the top of the DCU Menu. With the Set Channel button the user can set a new value for the DCU I2C hardware address, CCU address and I2C channel for the selected DCU. With the Set Default Channels (All DCUs) button the user restores the default DCU I2C hardware address, CCU addresses and I2C channels for all DCUs in the system.

The available registers on XROD to set the DCU settings through the I2C serial interface are the following (Figure 12):

3.9.1 **CREG, AREG, TREG (R/W Registers)**

The CREG (Control Register), REG (Auxiliary Register) and TREG (Test Register) are all read/write registers.

3.9.2 **SHREG, LREG (Read Only Registers)**

The SHREG (Status and Data High Register) and LREG (Data Low Register) are read only registers.

XROD also provides other DCU options which make use of these registers. The Reset DCU button sends a software reset of the DCU R/W registers (by writing a “1” into bit 6 of CREG (CREG<6>). An acquisition on a particular ADC channel can also be started with the Start Acquisition button (by writing a “1” into bit 0 of CREG, CREG<0>). The user should specify one of the eight possible ADC input channels. The Read button reads the data from the acquisition.

The user can set the DCU registers for the selected DCU by clicking on the Set button at the bottom of the screen. The settings for the selected DCU can be applied to all DCU’s by clicking on the Set All DCUs button. The Set Defaults (All DCUs) button sets the
defaults for each DCU. With the $DCU \leftarrow$ and $DCU \rightarrow$ buttons one can visualize the settings for each DCU.

### 3.10 The FED Menu

From the FED Menu (Figure 13) the user has access to up to 3 PMC-FED cards. The FED (Front-End Driver) digitizes the data coming from the APVs and transmits it to the DAQ system. The PMC-FED [11] is a FED prototype implemented as an 8 ADC channel PCI Mezzanine Card (PMC). This prototype has electrical inputs and is capable of digitising 9 bits at clock speeds between 2 and 40 MHz. The data in the PMC-FED is stored in DPM (Dual Ported Memory) synchronous memories and is capable of buffering the raw data from approximately 250 APV frames.

The status (enable/disable) of the 3 PMC-FEDs in the system is shown at the top of the FED Main window. Depending on the loaded configuration file (which defines the hardware configuration of the system), between one and up to three PMC-FED’s might be enabled.

The FED device number for each FED in the system can be changed to a new value or restored to the default one with the Set and Set Default Device buttons respectively, for each FED subpanel window.

The available registers on XROD to handle each of the three available PMC-FEDs on the FED subpanel windows are the following (Figure 13):

#### 3.10.1 FED Clock Settings

The clock is used to drive all the logic circuits of the FED and must always be running. There are two possible clock sources: PCI (internal clock at 33 MHz) or Front Panel (LVDS lines). A delay can be introduced into the clock signal path (in 10 steps of 2.5 ns for a total of 25 ns) which allows the phase of the clock relative to the data to be adjusted in order to obtain the optimum sampling point at the ADC.

#### 3.10.2 FED Trigger Settings

There are two possible trigger sources for the FED:

- **External Front Panel LVDS hardware triggers** (with a trigger pulse width of 25 ns), which come from the TSC board. This trigger source is available with “Scope Mode” and “Header Finder” trigger modes (see below).

- **Software triggers**, which are only available when the FED trigger mode is set in “Test Mode”, see below).

The FED can also be set to operate in three different trigger modes:
• **Scope Mode:** in this mode the FED uses hardware external triggers received from the TSC. The data capture starts a programmable number of clock cycles after the FED receives a trigger (called FED latency, see Section 3.2.5 in the *TSC Menu*), and continues for a programmable number of samples. In Scope Mode there is no data to readout. The output of the APV is at the logic 0 level, with synchronization pulses (tick marks) every 70 clock cycles (in 20 MHz APV readout mode, default) or 35 clock cycles (in 40 MHz mode).

• **Header Finder Mode (or Frame Finding Mode):** this mode permits ADC data capture to be triggered on recognition of a header word which accompanies the APV data stream (frame) itself rather than on the external trigger, and continues until the frame ends. A data set is made up of four parts:
  
  o A digital header (three bits, all logic 1).
  o A digital address (8 bit number, with MSB first, defining the column address used to store the signal when the chip is triggered).
  o An error bit (normally set in logic 1. If an error occurs in the APV internal logic, the bit is switched to logic 0).
  o An analog data set (128 samples).

• **Test Mode:** in this mode triggers are generated by software (external triggers are disabled).

The PMC-FED trigger is implemented as “Start Digitization”. A trigger pulse (either an external trigger from the TSC board or a software trigger) during a digitization run causes a pre-set number of samples to be digitized after a latency (number) of clock cycles and stored in the DPM.

### 3.10.3 FED ADC Channels

The FED 8 ADC channels are grouped into 4 pairs. The outputs of each pair can be enabled or disabled. Normally all channels should be enabled.

### 3.10.4 FED ADC Parameters

On receipt of a trigger (either external from the TSC or software) the data from a pre-set number of samples is captured in the DPM. The data from triggers are stored in the DPM in consecutive, contiguous buffers. The number of samples per event can be selected by the user (*Samples per Event*) but note that only certain sample sizes are permitted and illegal sample sizes might result in readout errors (see FED manual [11]). Note also that the data from the 8 ADC channels of each sample are interleaved. Therefore it is not possible to suppress the readout from individual ADC channels.

The ADC sample frequency can also be changed by the user (*Downsample*). If *Downsample* is disable the sampling is done for every clock. If enabled, the sampling is done for every second clock (in this case the *Samples per Event* should be adjusted accordingly).
3.10.5 FED FIFO Info and Counters

The occupied buffers window shows the number of occupied buffers, i.e., the number of pending events for readout (the buffer occupancy is reset to 0 at the start of each run). The purged buffers button clears all pending events in the DPM by flushing the PMC-FED FIFO. The occupied buffers counter will not be reset to 0 until the start of a new run.

The FED incorporates two event counters which are enabled during a digitization run. The Bunch Crossing Counter counts clock cycles and the Event Number Counter counts triggers. The APV Counters window shows...

3.10.6 FED Trigger Throttle

Events received when all buffers are occupied will overwrite previous events. The trigger throttle output is used to prevent this scenario. If the number of occupied buffers exceeds a programmable limit (Throttle Level) a hardware signal line can be generated to inhibit further triggers. The user can enable/disable the trigger throttle output. If trigger throttle is enabled and the buffer occupancy is greater than the Throttle Level value, the trigger throttle output is asserted.

XROD does not use this functionality and instead uses a software throttle logic during DAQ runs to prevent buffer overflows.

3.10.7 FED APV Parameters (FED Digital Thresholds)

A FED frame consists of the data from two APVs time-multiplexed together in alternate 40 MHz clock cycles. A frame begins with a digital header consisting of $2 \times 3$ successive high signals, followed by a pair of 8 bit APV pipeline addresses and a pair of error bits. This is followed by the analogue data from the $2 \times 128$ silicon strips. In Frame-Finding mode, the FED recognises from the data stream itself that a new APV frame has arrived.

The FED APV Parameters window allows the user to select the High and Low Threshold states in the APV digital output. These values are used in Frame Finding Mode to find the header which comes from the APV data stream. They should be determined from the baseline and amplitude of tick marks taken in Scope Mode (FED calibration run, see Section 3.11.1). These low and high levels should be monitored since they may drift as a result of instabilities in the laser drivers.

Other settings available in the FED APV Parameters window are the timeout length for frame finding recognition (Frame Timeout), the timeout length for tick recognition (Tick Timeout), and the number of samples which contain valid data in buffer (Frame Size).

The user can set the FED registers for the selected FED by checking on the Set this FED button at the bottom of the screen. The settings for the selected FED can be applied to all FEDs by clicking on the Set All FEDs button. The Set Defaults (All FEDs) button sets the
defaults for all FEDs. The Write All Registers and Read All Registers buttons write and read, respectively, the present register settings for the selected FED.

### 3.11 The DAQ Menu

From the DAQ Menu the user access five other scan submenus: the Noise Scan, the Timing Scan, the Pulse Shape Scan, the Gain Scan, the Optical Scan and the DCU Scan submenus. In all cases, at the top of the DAQ subpanel menu, the number of readout data events and the number of readout errors is always shown. A readout error is defined in Section 3.10.1 (Error Summary submenu). Also shown at the top of the DAQ window is the status of different FED related counters which are:

- **FED trigger counter**: these are the number of triggers arriving to the FED from the TSC card.
- **FED frame counter**: these are the number of frames found by the FED. The counter updates only when the FED is in Frame Finding Mode and an APV frame is found. In these conditions, the FED frame counter should be equal to the FED trigger counter.
- **FED buffer counter**: these are the number of events stored in the FED buffer FIFOs. Reading out events from the FED buffers frees the DPM memory occupied by these events. The number of events in the FED buffer counter plus the number of readout events should be the same as the number of events in the FED trigger counter.
- **TSC counter**: this is the TSC counter showing the number of TSC triggers sent to the FEC and FED boards.
- **Readout events and readout errors counters** for the selected FED.

The FED board for which all the above related counters are shown can be changed from the FED selection button.

The FED is designed to be readout in parallel with data capture. If the trigger rate is higher than the readout rate (the readout rate is limited by the computer bus speed and the online monitoring activity), the number of events stored in the FED FIFO buffers might overflow. This usually happens after approximately 680 events. If the FIFO overflows the buffer management breaks down and the run must be stopped and restarted. One common cause of overflow is caused by a missing external trigger. If a run is started (with external triggers selected) and the external trigger is missing (e.g. cable removed) a large number of spurious triggers are received which immediately overflows the FED buffers. XROD handles this situation (buffer overflow) by either disabling triggers into the FED or by purging all pending events in the DPM (by flushing the FED FIFO).
3.11.1 Noise Scan

From the *Noise Scan* submenu (Figures 14-17) the user can start a pedestal run with either TSC internal triggers or external triggers arriving to the TSC. The *Start* and *Stop* buttons start and stop the run respectively. When a run starts XROD automatically perform the following sequence:

1. Triggers are inhibited.
2. The FEC TTCRx and FEC drivers are initialized.
3. The I2C and PIO channels of the CCU are enabled.
4. A CCU reset to all modules in the system is sent.
5. All CCU I2C channels in the system are initialized and all front-end chip register settings are written according to the values read from the corresponding XROD menus (PLL, MUX, APV, and AOH).
6. The FED registers are written according to the *FED Menu* settings. Every enabled FED in the system is initialized with these settings.
7. The TSC trigger registers are written according to the *TSC Menu* settings. The TSC starts sending triggers.
8. FEDs start digitizing.
9. An APV and FED soft reset is sent to synchronize all FEDs in the system.

The user should check, before a run with TSC internal triggers starts, whether the FED trigger mode is set to either Frame Finding Mode or Scope Mode in the *FED Menu*. In Scope Mode the APV and FED latencies of the *TSC Menu* are set automatically to values of 500 and 100 clock cycles, respectively. This will assure that the FED trigger arrives long time before the APV reading, and the acquired data will not be polluted by any APV frame. Only APV baselines and ticks will thus be integrated. Running in Scope Mode can be useful to determine the FED low and high digital thresholds used in Frame Finding Mode to find APV headers (FED calibration run). When running with external triggers the FED is automatically set to Frame Finding Mode, and the user should check the timing for the signal by adjusting the APV latencies in both the *TSC Menu* and *APV Menu*.

The user has access to several real-time online distributions while data is being taken. These are the following:

*Frames*

The *Frames* submenu (Figure 14) shows the frame data for each of the FED channels defined in the system. The online distribution shows the digitized samples (in ADC counts) from FED frames (if running in Frame Finding Mode) or APV tick marks (if running in Scope Mode) as a function of time (clock cycles). Every FED laser channel contains the information from 2 multiplexed APV chips. A FED frame consists of a
digital header with 2×3 successive high signals, followed by a pair of 8-bit APV pipeline addresses and a pair of error bits. This is followed by the analogue data from the 2×128 silicon strips. Note that due to the structure of the analogue multiplexer the order that channels are readout through the analogue output is not consecutive.

Figure 14 shows an example of an online XROD frame distribution. The histogram shows the data for the first 400 samples by default. After the header and data from the APVs, an APV tick mark is also seen. The X and Y scale ranges can be changed at any time with the Set New Axis Scales button. The user can set the FED number and FED channel number to monitor at any moment during the run with the $FED \leftarrow$, $FED \rightarrow$, and $\leftarrow$ Channel, Channel $\rightarrow$ buttons, respectively.

Pedestals and Noise

The Pedestals and Noise submenus (Figure 15) show the instantaneous pedestal, the total RMS noise, the differential noise, and the CMS common mode noise substracted distributions (see [1] for a definition of these quantities) in ADC counts as a function of strip channel number, and for a selected silicon detector module (512 strips, from 0 to 511, for a module with 4 APVs, and 768 strips, from 0 to 767, for a module with 6 APVs).

Figure 15 shows an example of an online XROD noise distribution. The data shown has been taken with TSC internal triggers. An expanded view of the strips can be seen with the Set New Axis Scales button. The user can change the silicon detector module to monitor with the Module $\leftarrow$ and Module $\rightarrow$ buttons.

Pipeline Cells

The Pipeline Cells submenu (Figure 16) shows the pipeline address distribution for the 192 available cell address locations (from 0 to 191) for every APV chip in the system.

Figure 16 shows an example of an online XROD pipeline cells distribution. The data has been taken with external random triggers arriving to the TSC. The user can change the APV to monitor with the $APV \leftarrow$ and $APV \rightarrow$ buttons. In order to scan the whole pipeline, the reset status bit of the TSC control register (TSC Menu) must be set to OFF (no resets should be sent during triggers). Otherwise, sending a RESET101 sequence (reset status bit set to ON) reinitializes the pipeline for every event and the same pipeline location would be observed.

Clusters

The Clusters submenu shows online cluster distributions filled only when operating the system with external triggers. When running with external triggers (cosmics, $\beta$-source) a fast and simple online cluster algorithm can be used to find signal clusters on the silicon modules. Clusters are calculated and online histograms filled only when the Find Cluster button is checked. Two online histograms are shown: the cluster strip position distribution (as a function of strip number), and the cluster charge distribution (in ADC counts).
counts). Both distributions are shown per silicon detector module. The user can change
the detector module to monitor with the Module ← and Module → buttons.

When starting a run with external triggers and cluster finding, a special pedestal run is
taken first automatically with internal triggers. If the Find Clusters button is not checked,
the cluster finding algorithm is not applied and no pedestal run will be taken. The number
of events taken in this pedestal run is specified with the Pedestals button. The cluster
algorithm starts by finding first a seed channel in the detector module with a charge
above a Seed Cluster Charge value (in $\sigma$ RMS noise units). The adjacent strips may be
added to the seed channel by checking the Add Neighbours button. The strip neighbours
charge must be above the Neighbours Charge value (also in $\sigma$ RMS noise units). The
total charge of the cluster should be above the Total Charge value. The number of
detector module clusters found and the total number of clusters found in the run are
shown at the bottom of the cluster subpanel.

**Error Summary**

The Error Summary submenu (see Figure 17) shows a summary of the total number of
events readout and the total number of events with readout errors. Those number are
shown in total and for each individual FED in the system. A readout error is defined as an
event which satisfies, at least, one of the following conditions:

- The bunch crossing number is different between the different FEDs defined in the
  system.
- The event number is different between the different FEDs defined in the system.
- The cell pipeline address is different between the different APVs defined in the
  system.
- The APV error bit is set to zero in any of the APVs defined in the system.

### 3.11.2 PLL Timing Scan

The PLL Timing Scan submenu (Figure 18) provides an automatic way to find the correct
PLL settings for each detector module in the ROD. The PLL Timing Scan is based upon
measurement of APV tick marks for different PLL settings and a fixed digitization time
in the FEDs. XROD sets the FEDs trigger mode automatically in Scope Mode when the
run starts. The user specifies the begin, end and number of steps of PLL fine delays. The
online distribution showed in the PLL Timing Scan submenu shows the tick mark
mapping for each FED in the system (8 channels).

### 3.11.3 FED Timing Scan

The FED Timing Scan submenu (Figure 19) provides an automatic way to find the optimum FED sampling point for the data coming from the APVs. It should be performed
once the PLL time alignment scan is done and the PLL settings for each detector module
corrected. The optimum FED sampling point timing is based on measurements of APV
ticks and is controlled by:
- The TSC FED clock delay, which is fine tunable in steps of 1 ns (from 0 to 24 ns).
- The FED clock delay, which allows the phase of the FED clock relative to the data to be adjusted in steps of 2.5 ns (from 0 to 25 ns).

As in the case of the Optical Scan (see later in Section 3.11.5) the FED Timing Scan is based upon measurement of APV tick marks. XROD sets the FEDs trigger mode automatically in Scope Mode when the run starts. The FED Timing Scan starts by skewing the FED clock for every TSC FED delay according to user defined values (start of scan, end of scan, and number of scan points for both the TSC clock FED delay and the FED clock delay wrt data). This allows to map the image of the ticks for each TSC FED delay value. The online distribution showed in the FED Timing Scan submenu shows the tick mark mapping for a particular TSC FED delay value as a function of time (the default scale in the plot covers 2.5 µs, enough to show at least one tick mark from the APVs, which are sent every 1.8 µs). The sampling point should be picked for FED skew clock delays close to the back edge of the tick to ensure the system has settled for sampling. Any time difference in arrival of the ticks from different FED channels should be corrected with the PLL settings of the detector module hybrids (see PLL Menu in Section 3.5).

### 3.11.4 Pulse Shape Scan

From the Pulse Shape Scan submenu (Figure 20) the user can start a calibration test pulse shape scan. A test pulse shape scan is used to reconstruct the analogue waveform coming from the shaper output of the APVs. The pulse shape scans also allow for a verification of the signal shape and amplitude response of the full readout chain. The scan consists in reading the analogue output from a single channel while changing the phase of the calibration pulse with respect to the 40 MHz clock. The scan is defined by:

- An APV latency scan (using the APV latency register) providing a coarse resolution pulse shape mapping with steps given by clock cycles (25 ns). The beginning of the APV latency scan should be selected to match approximately the calibration latency value of the TSC sequencer register.
- A calibration delay scan (using the APV Csel register) for each APV latency point, and which provides a fine resolution pulse shape mapping with steps given by 3.125 ns units.

Each scan is repeated for the selected group of channels where charge is injected. These are a total of 8 groups (named group 0 to 7) of 16 channels each (Cdrv APV register, see Section 3.8.5).

The total number of events taken per scan point, the calibration pulse amplitude value (Ical), and the APV mode of operation (peak, deconvolution or multimode) can also be set directly from the Pulse Shape Scan submenu. The rest of APV settings (and other front-end chip settings) are readout from the corresponding menus before the scan begins when the Start button is pressed. Of particular importance for the user is to check the
“Cal Inhibit” bit of the APV Mode register (in the APV Menu) is set to OFF for every APV defined in the system. The scan can be stop at any moment with the Stop button.

The gain scan is performed with internal TSC triggers. At every scan point a reset sequence (101) is sent to all APVs of the system automatically.

There are two online distributions available to the user while data is being taken. These are:

- The pulse shape scan results shown for the 128 channels of an APV (APV submenu). The distribution shows the mean number of ADC counts (over the number of events per scan point) as a function of the scan point. With the $\Leftarrow$ APV and $\Rightarrow$ APV buttons the user selects the APV to monitor.

- The pulse shape scan results shown per channel (Channel submenu). The distribution shows the mean number of ADC counts (over the number of events per scan point) as a function of the scan point. With the $\Leftarrow$ APV, $\Rightarrow$ APV and $\Leftarrow$ Channel, $\Rightarrow$ Channel buttons the user select the APV and channel number to monitor, respectively. To show the results for a particular channel, select it and use the Go button.

### 3.11.5 Gain Scan

From the Gain Scan submenu (Figure 21) the user can start a calibration test pulse gain scan. A gain scan is usually used to test the linearity of the circuit. The scan starts with a calibration test pulse amplitude scan where the steps are given in calibration pulse Ical units (625 electrons, see [9]). The user can also select the group of channels where to inject charge through the scan (given by the Cdrv APV register). There are a total of 8 groups (0 to 7) of 16 channels each.

The total number of events taken per scan point and the calibration delay value (Csel APV register) can also be set from the Gain Scan submenu. The rest of APV settings (and other front-end chip settings) are readout from the corresponding menus before the scan begins when the Start button is pressed. Of particular importance for the user is to check the “Cal Inhibit” bit of the APV Mode register (see the APV Menu) is set to OFF for every APV defined in the system (XROD automatically disables it on a gain scan). The scan can be stop at any moment with the Stop button.

The gain scan is performed with internal TSC triggers. There are two online distributions available to the user while data is being taken. These are:

- The gain scan results shown for the 128 channels of an APV (APV submenu). The distribution shows the mean number of ADC counts (over the number of events per scan point) as a function of the calibration pulse Ical value. With the $\Leftarrow$ APV and $\Rightarrow$ APV buttons the user selects the APV to monitor.

- The gain scan results shown per channel (Channel submenu). The distribution shows the mean number of ADC counts (over the number of events per scan point) as a function of the calibration pulse Ical value. With the $\Leftarrow$ APV, $\Rightarrow$ APV
and &lt;Channel, Channel &gt; buttons the user select the APV and channel number to monitor, respectively. To show the results for a particular channel, select it and use the Go button.

3.11.6 Optical Scan

From the Optical Scan submenu (Figure 22) the user can start an analogue optical link characterization through an automatic scanning of laser optohybrid bias and gain settings. The optical scan is used to find the best operating conditions of the AOH bias and gain settings for the laser diodes. The optical scan works by automatically setting the FEDs trigger mode in Scope Mode (the FED uses hardware triggers from the TSC). The APV and FED latencies of the TSC Menu are also set automatically to values of 500 and 100 clock cycles, respectively. This will assure that the FED trigger arrives long time before the APV reading, and the acquired data will not be polluted by any APV frame. Only APV baselines and ticks will thus be integrated.

The optical scan starts by scanning on AOH Bias and Gain values defined by the user. The laser diodes bias currents can be set with values between 1 and 127 (7 bit values). Note that when the bias is set to zero the power-down function is activated and the laser driver will then be disabled (useful for reducing the power consumption and noise of a non-used or defective channel). The laser driver gains can be set between 0 and 3 (2 bit values). The total number of events taken per scan point is set from the Number of Events button. Every event consists on the number of samples defined in the FED Menu.

There are two online distributions available to the user while data is being taken:

- For every gain and bias scan point, the histogram in the Baseline Ticks submenu shows the distribution of baselines and tick marks (in ADC counts) for every FED and FED channel (or analogue optical link) in the system. With the FED &lt;, FED &gt;, and Channel &lt;, Channel &gt; buttons the user select the FED board and FED channel to monitor, respectively.
- The histogram in the Height submenu shows the tick amplitudes as a function of the laser bias I2C settings for every FED channel (or analogue optical link) in the system. The tick amplitudes are calculated by fitting the baseline and tick distributions to Gaussian functions and subtracting their mean values. With the FED &lt; and FED &gt; buttons the user selects the FED board to monitor. With the Gain &lt; and Gain &gt; buttons the user select the tick amplitude distributions for every gain I2C settings in the scan. The optimal settings should be obtained by the lowest bias settings for full amplitude.
References


Figure 1: XROD Main Menu.

Figure 2: XROD Configuration window.
1 Module (4 APVs)
#
# TSC Configuration:
#===================
TSC Device: 0
#
# FEC Configuration:
#===================
FEC Device: 0
#
# CCU Configuration:
#===================
CCU Address: 36
CCU Type: 0
#
# FED Configuration:
#===================
FED Device: 0
FED Clock Delay: 0
#
# DCU Configuration:
#===================
CCU DCU: 36
I2C DCU: 1
Address DCU: 0
Type DCU: 2
#
# PLL Configuration:
#===================
CCU PLL: 36
I2C PLL: 1
Address PLL: 68
Latency PLL: 20
L1Delay PLL: 1
#
# MUX Configuration:
#===================
CCU MUX: 36
I2C MUX: 1
Address MUX: 134
Resistor MUX: 255
#
# OPTO Configuration:
#====================
CCU OPTO: 36
I2C OPTO: 1
Type OPTO: 0
Address OPTO: 15
Chan1 OPTO: 1
Gain1 OPTO: 2
Bias1 OPTO: 8
Chan2 OPTO: 2
Gain2 OPTO: 2
Bias2 OPTO: 8
Chan3 OPTO: 3
Gain3 OPTO: 2
Bias3 OPTO: 8
#
# APV Configuration:
#===================
CCU APV: 36 36 36 36
I2C APV: 1 1 1 1
Address APV: 64 66 72 74
Latency APV: 100 100 100 100
MUXresistor APV: 2 2 2 2
AnalogBias APV: 1 1 1
Inverting APV: 1 1 1 1
CalInhibit APV: 1 1 1 1
OneSample APV: 1 1 1 1
PeakMode APV: 1 1 1 1
HighFreq APV: 0 0 0 0

Figure 3: XROD configuration file for one silicon detector module with 4 APVs (xrod_1module_4apv.conf).
Figure 4: Set Number and Type of Modules (top) and RODs to Readout (bottom) windows.

Figure 5: XROD TSC Menu.
Figure 6: XROD FEC Menu.

Figure 7: XROD CCU Menu.
Figure 8: XROD PLL Menu.

Figure 9: XROD MUX Menu.
Figure 10: XROD OptoHybrid Menu.

Figure 11: XROD APV Menu.
Figure 12: XROD DCU Menu.

Figure 13: XROD FED Menu.
Figure 14: XROD DAQ Menu: Noise Scan with Frames subpanel view.

Figure 15: XROD DAQ Menu: Noise Scan with Noise subpanel view.
Figure 16: XROD DAQ Menu: Noise Scan with Pipeline Cells subpanel view.

Figure 17: XROD DAQ Menu: Noise Scan with Error Summary subpanel view.
Figure 18: XROD DAQ Menu: PLL Timing Scan.

Figure 19: XROD DAQ Menu: FED Timing Scan.
Figure 20: XROD DAQ Menu: Pulse Shape Scan.

Figure 21: XROD DAQ Menu: Gain Scan.